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Hot Hole-Induced Device Degradation by Drain Junction Reverse Current

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Components of drain leakage currents in the off-state of MOSFET are gate-induced drain-leakage (GIDL) and drain junction reverse currents. Device degradation phenomenon and mechanism by GIDL have been well known, but those by drain junction reverse current (I_{DJR}). have not. In this paper, device degradation mechanisms by drain junction reverse current in the off-state were studied through *I-V* curves (V_{TH} and mobility) and charge pumping technique.

Experience & Result

N-channel MOSFETs (N-MOSFETs) were fabricated, which were used as the high-voltage core circuit of flash memory chip. The gate oxide (SiO_2) was grown by oxidation to a thickness of 140 Å. The nitride spacer length was 0.14 µm, and the gate width and length were 10 and 0.44 µm, respectively. The overlapped length between the gate and the drain was 0.0315 µm.

A variety of drain current measurement configurations were shown in Fig. 1, and each measured drain currents from Fig. 1 were shown in Fig. 2. The drain current curves of Fig. 2 (a) and (b) are laid on the same line, and, I_{GIDL} pictured in Fig. 2 (c) occurs when V_D > 13 V; its value is very small compared with the drain currents of Fig. 2 (a) and (b). In conclusion, it is possible to ignore I_{GIDL} in cases of which the V_D is less than 13 V, and the drain currents of Fig. 2 (a) and (b) are simply drain junction reverse current (I_{DJR}).

Figure 3 shows gate current according to drain voltage under the measurement conditions of Fig. 2 (a). The gate current has a negative value, which means holes were injected to the gate under I_{DJR} stress of Fig. 1 (a).

Device degradation after I_{DJR} stress was evaluated by changes of V_{TH} and mobility. It is well known that the decrease of V_{TH} is influenced by trapped holes, and the decrease of mobility is influenced by interface traps. As shown in Fig. 4, as stress V_D increased, V_{TH} and mobility decreased, which means that hole trapping and interface traps were generated (stress condition: V_D=11.6 V, 100 s with Fig. 1 (a) condition). In addition, the presence of the interface traps implies that drain off-leakage current (I_{off}) can increase. Figure 5 shows the I_{off} increased by interface traps after stress.

Device degradation phenomenon by I_{DJR} is similar to that by I_{GIDL}. Namely, holes generated in the drain junction depletion region were injected into the gate and trapped into the gate oxide, reducing V_{TH} and mobility (μ_{eff}). However, the location of charge injection is somewhat different between I_{GIDL} and I_{DJR}. In the case of I_{GIDL}, electron-hole pairs are generated in the gate-drain overlap region; in the case of I_{DJR}, however, electron-hole pairs are generated in the drain junction depletion region. Figure 6 shows the lateral profile of trapped holes extracted from the charge pumping method after stress (I_{DJR} stress was V_D = 11.6 V for 100 s under the conditions of Fig. 1 (a), and I_{GIDL} stress was V_D = 15 V for 100 s under the conditions of Fig. 1 (c)). Here, the absolute value of number of trapped holes (N_{ot}) according to the stress type is not important because stress conditions were different between I_{DJR} and I_{GIDL} stress. Electron-hole pairs by I_{DJR} are most likely to generate at the metallurgical drain junction where the lateral electrical field is greatest, and electron-hole pairs by I_{GIDL} is likely to generate at the gate-drain overlap region. Therefore, the point at which N_{ot} by I_{DJR} stress increases is closer to the channel than that of I_{GIDL}, as shown in Fig. 6.

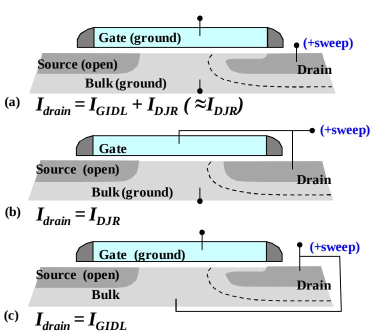

Fig. 1. Drain current measurement configurations.

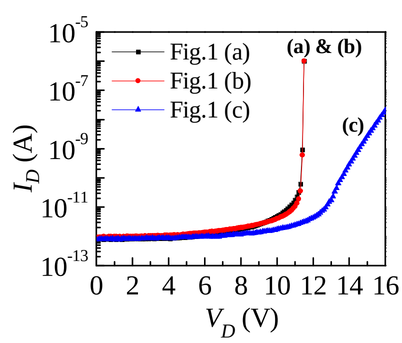

Fig. 2. Drain currents under measurement conditions depicted in Fig. 1.

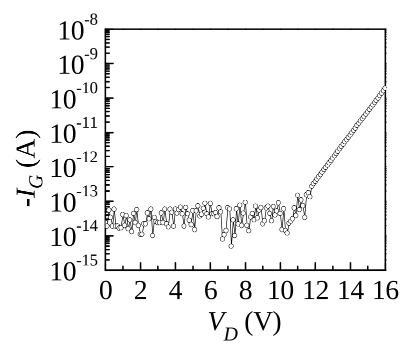

Fig. 3. Gate current according to drain voltage under the measurement conditions of Fig. 2 (a)

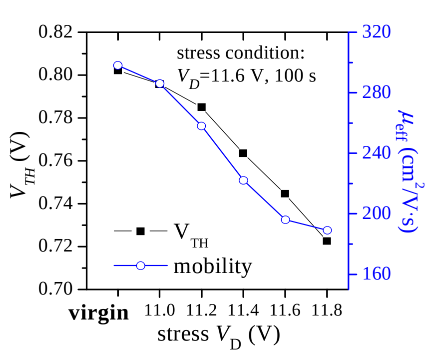

Fig. 4. Degradation of threshold voltage (V_{TH}) and mobility (μ_{eff}) after I_{DJR} stress.

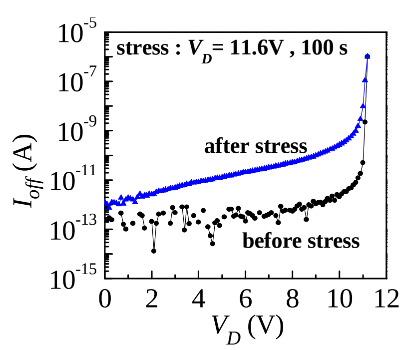

Fig. 5. Degradation of drain off-leakage current (I_{off}) after I_{DJR} stress

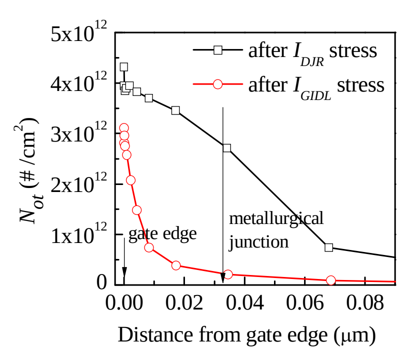

Fig. 6. Lateral profile of trapped holes extracted using the charge pumping method after I_{DJR} stress.