

## Low-Frequency-Noise-Based Oxide Trap Profiling in Replacement High-k/Metal-Gate pMOSFETs

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**1. Introduction.** There is currently a strong interest in the implementation of a replacement high-k/metal gate approach, offering a wider process window for the deposition of metal-oxide cap layers to tune the work function, and, hence the threshold voltage  $V_T$  [1,2]. One of the main concerns is to achieve a similar interface and oxide quality as for the standard gate first technology. Detailed studies have shown that both the interface state density, the low-field mobility and the reliability of the gate stack is largely preserved [1]. This was also confirmed by low-frequency (LF) noise measurements [3], which is a suitable tool for the study of near-interface border traps in the gate stack [4]. In fact, analyzing the frequency exponent  $\gamma$  of the  $1/f^\gamma$  spectra enables to extract some information on the general nature of the border trap density profile in the high-k oxide. The aim of the present paper is to report on the LF noise and the corresponding trap density profiles of HKMG last pMOSFETs with an Equivalent Oxide Thickness (EOT) of  $\sim 1$  nm. It is shown that for reference devices, the trap density increases with depth into the  $\text{HfO}_2$ , which confirms past results [5]. However, post-deposition exposure to a F-containing plasma etch changes the shape of the profile, evidencing the passivation of process-induced oxide traps by F [3,6].

**2. Experimental conditions.** The studied planar bulk pMOSFETs have been processed on 300 mm wafers, whereby the dummy gate is removed by HF etch. Next, a chemical interfacial oxide layer is grown in ozone, to create an  $\text{SiO}_2$  interfacial layer (IL), followed by 36 cycles of  $\text{HfO}_2$  by Atomic Layer Deposition (ALD). One wafer received a post-deposition 9 min  $\text{SF}_6$  plasma exposure to introduce F in the gate stack. This was followed by a 1 min anneal in  $\text{N}_2$  at 500 °C [6]. LF noise measurements have been performed as described earlier [3], on  $1 \mu\text{m} \times 0.170 \mu\text{m}$  pMOSFETs ( $\Delta L \sim 35$  nm) in linear operation ( $V_{DS} = -0.05$  V) and with the gate stepped from weak to strong inversion. The frequency exponent is analyzed following the approach originally proposed by Çelik-Butler and Hsiang [7].

**3. Results and discussion.** It is shown that the LF noise spectra are predominantly  $1/f^\gamma$ -like (flicker noise), with a normalized Power Spectral Density (PSD) following correlated number fluctuations. In other words, the flicker noise is due to gate-oxide trapping. In line with previous results, it is found that exposure to the F plasma reduces both the average PSD and the sample-to-sample spread [3,6]. In order to further exploit the noise spectra, the frequency exponent has been derived versus the gate voltage. Based on the fact that  $g = (\gamma - 1)\alpha_t$ , with  $\alpha_t$  the tunneling attenuation factor of the electron wave function into the oxide, one can approximate the normalized oxide trap density profile by  $N_{ot}(z) = N_{ot}(z=0) \exp(gz)$  [7]. Taking the value at  $V_{GS} \sim V_T$  yields the shape of the trap density profile at zero oxide field [4].

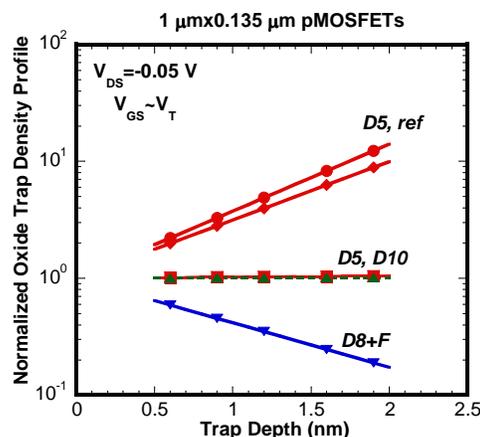


Fig. 1. Normalized trap density profile for two reference wafers (D5 and D10) and for a wafer, receiving a 9 min  $\text{SF}_6$  plasma etching to introduce F atoms in the gate stack (D8).

A typical example is shown in Fig. 1, combining data for two reference wafers and a pMOSFET exposed to F. First of all, it is clear that there exists some device-to-device variability in the oxide trap density profile: while some references exhibit a strong increase of  $N_{ot}$  with depth, other devices show a more or less constant profile. This means that not only the trap density but also the depth distribution can contribute to the noise variability.

A second fact which is obvious from Fig. 1 is that the F-passivated pMOSFET has a trap density profile which decays with distance from the Si/IL interface. This gives evidence of the passivating effect of F in the gate dielectric, by in-diffusion from the gate. So, not only the total trap density is reduced but this occurs more efficiently further away from the interface.

**4. Conclusions.** It has been shown that the exposure of HKMG last pMOSFETs to a  $\text{SF}_6$  plasma not only improves the LF noise by passivating a part of the oxide traps, at the same time, this passivation occurs more pronounced away from the interface. As a consequence, the frequency exponent of the flicker noise spectra changes from  $>1$  for the references to  $<1$  for the F-treated devices, at  $V_{GS} \sim V_T$ .

## References

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