Some strategic tracks to optimize routing of high speed signal transmission between memory and logic in 3D-IC stacks

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After LPDDR2 standard for low power DRAM (Dynamic Random Access Memory) and mobile memory applications, Wide IO is presented as a promising alternative solution face to new LPDDR3 standard because of its lower power consumption, lower latency, lower weight and package size and comparable bandwidth [1]. Rate of 12.8 GBps with 600 mW consumption power are expected [2]. Nevertheless Wide IO appears as the killing application for 3D needing the weighty technology breakthrough of advanced 3D integration developments.

Three 3D stacking strategies to develop Wide IO were evaluated to optimize electrical performances. The two first configurations consist in either a Face-to-Face (F2F) or a Face-to-Back (F2B) stacking of memory chip upon a processor using Cu-Pillars and Through Silicon Vias (TSVs). In the third configuration, memory chips and processor are simultaneously stacked upon a silicon interposer by Cu-Pillars. This interposer, using TSVs, is dedicated to the interconnect network between memory chips and processor and with the BGA (Ball Grid Array). Performances of Wide IO are impacted by these different 3D stacking strategies because 3D interconnects networks are specific in terms of interconnection length, 2D (Back End Of Line (BEOL) and ReDistribution Layer (RDL)) and 3D (TSV, Cu-Pillar) topologies.

In our works, electrical performances of Wide IO are predicted in terms of delay, bandwidth (maximal frequency) and signal integrity using eye diagrams for each 3D stacking strategy: F2F, F2B or interposer solution. Interconnect networks of these 3D ICs are constructed using a building block of accurate electrical models for each basic interconnect element (TSV, Cu-Pillar, RDL and BEOL interconnects). These electrical models, useable on a large frequency band to rigorously simulate the transmission of high speed signals in Wide IO, have been developed in [3].

Maximal transmission frequencies between memory chips and processor and between processor and BGA are evaluated for each stacking strategy and for several technological generation of 3D interconnects, ranging from low density TSVs with 60 µm diameter to high density TSVs with 3 µm diameter. As example, using a middle density technology with 10 µm diameter TSVs and with 20 and 55 µm diameters for Cu-pillar respectively between memory and processor, and between processor and BGA, it is shown that up to 9.9 GHz and 6.8 GHz frequencies can be carried out between memory and processor for respectively F2F and F2B stacks. These frequencies are reduced between processor and BGA because the impact of capacitive effects by Cu-Pillars. Interposer solution gives an attractive bandwidth for memory to processor communication, and for processor to BGA. These results are confirmed by a large study about signal integrity using eye diagrams, as shown on Fig. 1 for the interposer solution.

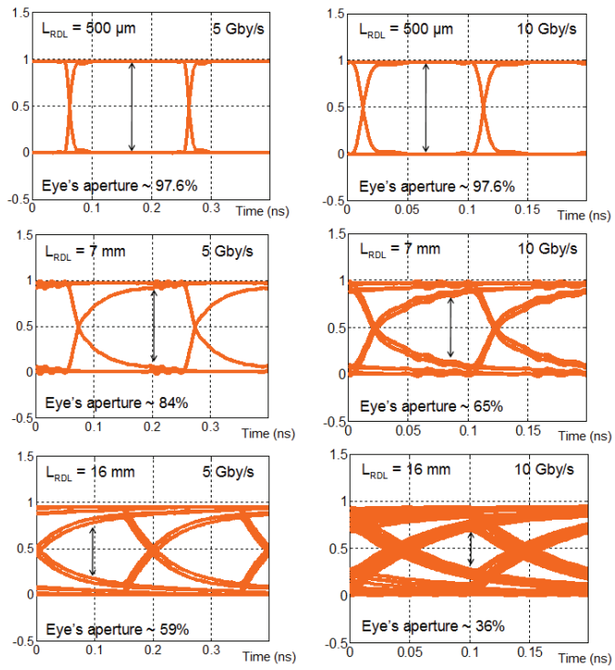

Fig. 1. Eye diagrams for data rates of 5 GBy/s and 10 GBy/s between memory and logic using interposer solution.

Yet roadmap objectives for Wide IO can be achieved with interposer solution using higher density TSVs. Although performances in term of rate of this interposer solution are lower than F2F ou B2F solutions, it provides also more routing flexibility and low cost.

In conclusion electrical performances of Wide IO are predicted and compared for several interconnect routing and 3D staking strategies versus technological generations for integration densities. Roadmap and design rules are proposed to optimize electrical performances and to achieve expected rate for Wide IO.

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