A Vertically Integrated Capacitorless DRAM Cell

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Inspired by the latch-up effect, a 2-port capacitorless, gate-free and vertical memory cell with a PNPN+R structure was demonstrated. Compared with the previous 2-port gateless memory cell Biristor [1], the new cell mainly uses positive feedback [2] as programing mechanism, and introduces a top layer R (resistor) for current restrain, operation voltages and currents is largely reduced. In this work, the fabrication, memory cell concept, operation mechanism, process variation, reliability and basic performances including the speed and retention time presented.

The cell structure compatible with CMOS is shown in Figure 1. Because of the vertical structure, F^2 cell area can be achieved. The cell was fabricated and its hysteric curve is shown in Figure 1. When V_{AC} increases in the forward direction, the memory cell stays at a low conductance (defined as Bit "0") until V_{AC} gets to V_{LU}. At V_{LU}, the positive feedback happens and the memory cell gets into a high-conductance state (defined as Bit "1"). Once latched up, a large number of charges were injected into the central 2 layers. The injected charges keep the cell latched and "1" is conserved within retention time.

The hysteric curves of cells uniformly located on the same 4-inch wafer are shown in Figure 2, which indicate a good process uniformity of the new cell. The fresh hysteric curve, curve after 1000 times -5V~5V~-5V static sweeps and curve after 6 months are shown in Figure 3, which shows good reliability of the new cell. A pulsed I-V performance is evaluated by use of measurement circuit and operational conditions shown in Figure 4. The memory cell exhibits a remarkably large sensing current ratio (I_{D1}/I_{D0}) of about 10^4 as shown in Figure 5. Such a large sensing current ratio can provide enough read margin for rapid read operation and avoid soft error. Like the traditional DRAM cell, the stored excess charges gradually disappear as a result of junction leakages and recombination. Retention time (Tr) is the longest time in which the cell can stay at "1". Tr of this fabricated memory cell is about 200ms. Unlike the conventional DRAM cell, the sensing current is not degraded with respect to the read time. Therefore, a multiple read becomes possible, as shown in Figure 6. Figure 7 shows that the memory cell works at a program and erase speed down to 200ns, which is our measurement limit. High-frequency performances were studied with calibrated simulation, results are shown in Figure 8, which indicate that this new memory cell can be operated at ns level. Figure 9 summarizes the features of the Biristor and the proposed cell with the same area. We can see that the program power and refresh power of the new cell were obviously reduced, which provide a better potential for practical application. Furthermore, the proposed memory cell has only two ports, so a stand-alone memory with cross-point structure [4] on a bulk wafer can potentially be exploited.

In a summary, we present a PNPN+R structure DRAM cell for high-speed, high-density and low power applications. The new cell is compatible with CMOS, showed a large sensing currents margin, an available retention time, good process uniformity and high reliability. The new memory cell can potentially find use in a broad range of memory applications.

[1] Jin-Woo Han et al., VLSI 2010. [2] J. F. Gibbons, TED, 1964. [3] Hyun-Jin Cho et al., IEDM 2005. [4] Jiale Liang et al., TED 2012.

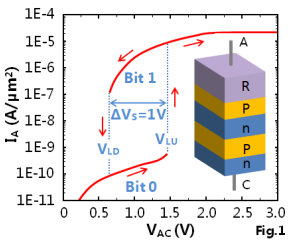

Fig.1

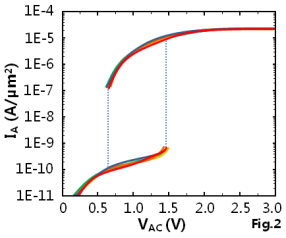

Fig.2

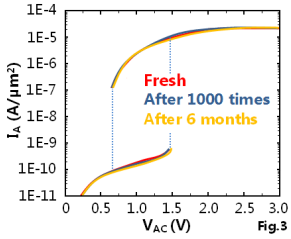

Fig.3

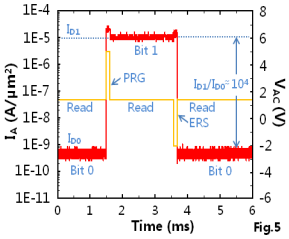

Fig.5

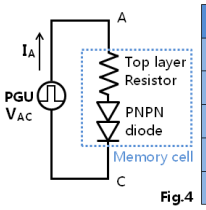

Fig.4

Operational conditions		
Program(V_P)	$V_P > V_{LU}$	5V
Erase(V_E)	$V_{LU} < V_E < 0$	-2V
Read(V_R)	$V_{LD} < V_R < V_{LU}$	1.4V
Hold(V_H)	$V_H = 0$	0V
Refresh(V_{Ref})	$V_{Ref} = V_R$	1.4V

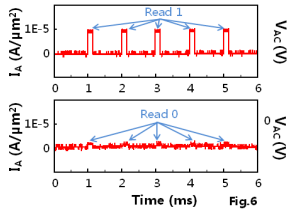

Fig.6

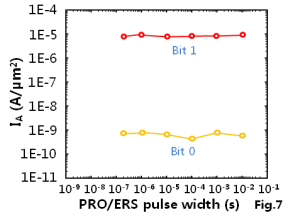

Fig.7

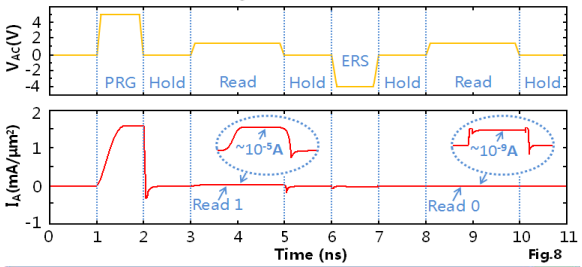

Fig.8

Comparison	Area	Speed	Retention time	Read current ratio	Program power (w/bit)	Erase power (w/bit)	Refresh power (w/bit)
Bristor	F^2	ns	Few 100 mSecs	~10^4	~3×10^{-3}	negligible	~1×10^{-3}
This work	F^2	ns	Few 100 mSecs	~10^4	~2×10^{-5}	negligible	~3×10^{-8}

Fig.9