InGaAs GAA Nanowire MOSFETs

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Recently, III-V MOSFETs with high drain currents (I_{ds}>1mA/μm) and high transconductances (g_m>1mS/μm) have been achieved at sub-micron channel lengths (L_{ch}), thanks to the better understanding and significant improvement in high-k/III-V interfaces. However, to realize a III-V FET at beyond 14nm technology node, one major challenge is how to effectively control the short channel effects (SCE). Due to the higher permittivity and lower bandgap of the channel materials, III-V MOSFETs are more susceptible to SCE than its Si counterpart. The scaling of planar devices stops at around 150nm L_{ch}. The dramatic increase in DIBL beyond 150nm indicates severe impact from 2D electrostatics. Therefore, the introduction of 3-dimensonal (3D) structures to the fabrication of sub-100nm III-V FETs is necessary. In this talk, we will review the materials and device aspects of III-V 3D transistors developed very recently [1-3]. We will also report some of new progress by demonstration of 20-80 nm channel length III-V gate-all-around nanowire MOSFETs with EOT=1.2nm and lowest SS=63 mV/dec [4]. The total drain current per pitch can be further enhanced by introducing 4D structures [5].

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