Effect of intermetal dielectric layer on the interpoly dielectric properties of nonvolatile memory devices

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ABSTRACT

This paper describes the influence of water-related species contained in intermetal dielectric layer on the interpoly dielectric properties of nonvolatile memory devices. P-TEOS layer used as an intermetal dielectric enhances degradation of interpoly dielectric of nonvolatile memory devices due to the water-related components contained in the layer.

INTRODUCTION

With the shrinkage of device dimensions, it becomes difficult to fill the gap between the metal lines without void formation and planarize surface topology using conventional silane-based plasma CVD SiO_2 (P-SiO_2). To solve this problem, plasma CVD using tetraethyl orthosilicate (P-TEOS) has been used because of its better step coverage. However, such dielectric layers with good step coverage usually contain a large amount of water-related species and degrade the hot-carrier immunity of NMOSFETs[1-4]. The amount of interface traps generated by hot carrier injection is proportional to the concentration of water-related species diffusing from intermetal oxides adjacent to Si/SiO_2 interface [3]. It is known that water-related minute impurities such as H, OH introduced into oxides create additional Si-H and Si-OH bonds at the Si/SiO_2 interface [5]. In addition, it has been investigated that the main species enhancing degradation is H_2O diffusion [3].

In the present work, we have evaluated the influence of the intermetal layer on the interpoly dielectric properties of nonvolatile memory devices.

EXPERIMENTS

Two type intermetal dielectric structures were used to investigate the effect of intermetal layer. The dielectric films were deposited on the 1st-metal layer using P-TEOS. The dielectric structures consisting of P-TEOS on 1st-metal are listed in Table I. Since the total amount of water-related components is proportional to the volume of P-TEOS, the amount of water-related components contained in the film was controlled by the thickness of P-TEOS [1].

Table I Dielectric structures used in this study.

SAMPLE	P-TEOS (nm)
A	400
B	800

The interpoly dielectric used in this study was 20nm oxide-nitride-oxide (ONO) multi-layered film of nonvolatile memory cells. Conventional double-polysilicon stacked-gate were deposited for interpoly dielectric formation. To evaluate the ONO film properties, patterned poly-Si capacitor structure was used.

RESULTS AND DISCUSSION

Fig. 1 shows I-E characteristics and the trapping effect of ONO stacked film (sweep range: 3~15V, 85℃). At the 2nd sweep measurement, leakage current of sample B is smaller than that of sample A due to the larger electron trapping during the 1st sweep measurement. These results show that amount of interface traps generated by electric field is proportional to the concentration of water-related species diffusing from intermetal oxides adjacent to bottom oxide/SiN interface of ONO film [6].

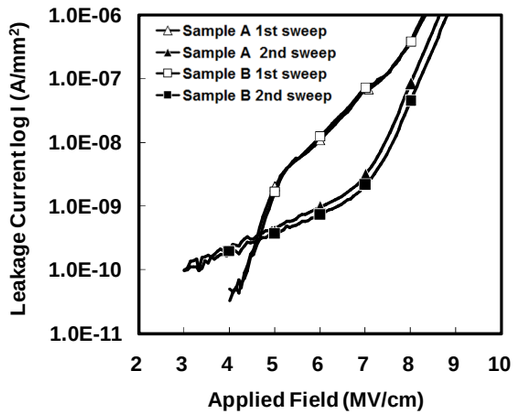

Fig.1 I-E Characteristics for ONO film on patterned poly-Si capacitor.

CONCLUSION

Intermetal dielectric layers such as P-TEOS which contain a large amount of water degrade the bottom oxide/SiN interface of interpoly dielectric due to the water-related components diffusing from intermetal oxides. Control of the amount of water contained in intermetal dielectric layer is necessary to enhance the interpoly dielectric properties of nonvolatile memory devices.

REFERENCES

[1] N. Shimoyama, K. Machida, K. Murase, and T. Tuchia, " Enhanced Hot-Carrier Degradation due to Water in TEOS/O_3-Oxide and Water Blocking Effect of ECR-SiO_2", *Symp. on VLSI Tech. Dig*., 1992, pp. 92-95.

[2] K. Shimokawa, T.Usami, S.Tokutou, N.Hirashita, M. Yohimaru, and M. Ino, "Suppression of the MOS Hot Carrier Degradation caused by Water desorbed from Intermetal Dielectric", *Symp. on VLSI Tech. Dig*., 1992, pp. 96-97.

[3] M. T. Takagi, I. Yoshii, and K. Hashimoto, " Characterization of Hot-Carrier Degradation of MOSFETs Enhanced by H_2O Diffusion for Multilevel Interconnection Processing", *IEEE IEDM Tech. Dig*., 1992, pp.703-706.

[4] E. Sakagami, N. Arai, H. Tsunod, H. Egawa, Y. Yamaguchi, E. Kamiya, M. Takebuchi, K. Yamada, K. Yoshikawa, S.Mori, "The impact of intermetal dielectric layer and high temperature bake test on the reliability of nonvolatile memory devices", *Proc. 32th IEEE IRPS*,1994, pp. 359-367.

[5] Y. Ohji, Y. Nishioka, K.Yokogawa, K. Mukai, Q. Qiu, E. Arai, and T. Sugano, "Effects of Minute Impurities (H, OH, F) on SiO_2/Si Interface as Investigated by Nuclear Resonant Reaction and Electron Spin Resonance" *IEEE Tran. Electron Devices*, vol.37,1990, pp. 1635-1642.

[6] S. Mori, Y. Kaneko, N. Arai, Y. Ohshima, H. Araki, K. Narita, E. Sakagami, and K. Yoshikawa, " Reliability study of thin inter-poly dielectrics for non-volatile memory application", *Proc. 28th IEEE IRPS*,1990, pp. 132-144.