Performance Enhancement Technologies in III-V/Ge MOSFETs

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MOSFETs using channel materials with low effective mass have been regarded as strongly important for obtaining high current drive and low supply voltage CMOS under sub 10 nm regime [1, 2]. From this viewpoint, attentions have recently been paid to III-V and Ge channels. This is because III-V semiconductors have extremely high electron mobility and low electron effective mass and Ge has extremely high hole mobility and low hole effective mass. Thus, one of the ultimate CMOS structures can be the combination of III-V nMOSFETs and Ge pMOSFETs [1-4].

In order to realize III-V/Ge CMOS, common gate stack and source/drain (S/D) formation technologies are important. Here, an ALD Al_2O_3 gate insulator and Ta metal gate were used for common gate stacks for InGaAs and Ge. This is because ALD Al_2O_3 can provide good MOS interfaces with InGaAs as well as Ge with post ECR plasma oxidation [5]. We have recently realized HfO_2/Al_2O_3 gate stacks with EOT of 1 nm or less for both InGaAs [6] and Ge [7], allowing us to simultaneously satisfy both thin EOT and good MOS interface properties as the common gate stacks. Particularly, as for the Ge gate stacks, ECR plasma post oxidation through HfO_2/Al_2O_3 is quite effective in realizing Ge gate stacks with EOT less than 1 nm with low D_{it} and resulting high electron and hole mobility in Ge MOSFETs [7], as shown in Fig. 1. Record high mobility Ge n- and p-MOSFETs with EOT of 0. 76 nm have been demonstrated by using $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks (Fig. 2).

Self-align Ni-Ge and Ni-InGaAs, which can be formed simultaneously for InGaAs nMOSFETs [8] and Ge pMOSFETs, were used as the metal S/D regions. Recently, we have realized 50-nm-L_g InGaAs-OI MOSFETs with Ni-InGaAs S/D on Si substrates (Fig. 3) by employing direct wafer bonding between InGaAs and Si substrates with ultrathin Al_2O_3 buried oxides (BOX) [9]. The good performance is confirmed in Fig. 4.

By utilizing these technologies, we have also demonstrated successful integration of InGaAs-OI nMOSFETs and Ge p-MOSFETs on a same wafer and their superior device performance [10]. We have found good transistor operation in both devices. High Ion/Ioff ratio of ~10^6 was obtained for InGaAs-OI nMOSFETs. The high electron and hole mobility of 1800 and 260 cm^2/Vs and the mobility enhancement against Si of 3.5× and 2.3× have been demonstrated for InGaAs-OI nMOSFETs and Ge pMOSFETs, respectively.

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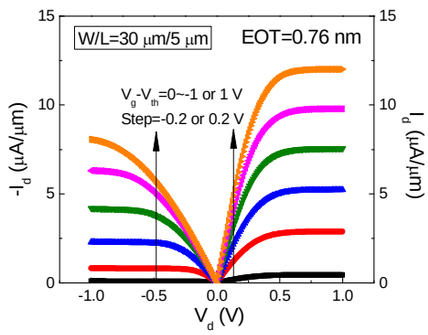

Fig. 1 The Id-Vd characteristics of the Ge p- and n-MOSFETs with HfO_2(2.2nm)/Al_2O_3(0.2nm)/GeO_x(0.35nm)/Ge gate stacks

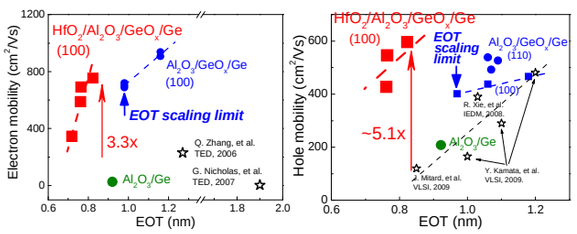

Fig. 2 The peak (a)electron and (b) hole mobility of the Ge p- and n-MOSFETs with $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks (red symbols) vs. EOT, compared with the Ge MOSFETs with Al_2O_3/GeO_x/Ge gate stacks (blue symbols) and the data reported in other previous researches

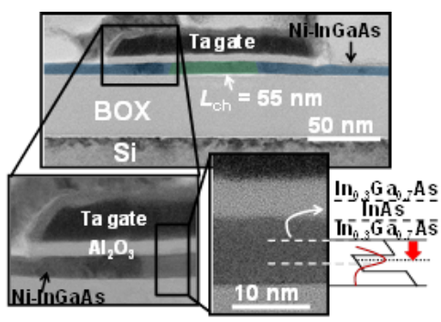

Fig. 3 A cross-sectional TEM image of the fabricated InAs-OI MOSFETs with a Lch of 55 nm, Tbody of 3/3/3 nm.

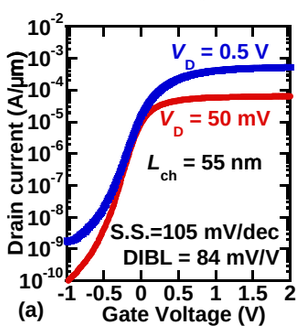

Fig. 4 The I_D-V_G characteristics of InAs-OI MOSFETs with T_{body} of 3/3/3 nm, T_{ox} = 6 nm. Good transfer and output characteristics were obtained due to thin channel thickness.