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Reliability of ALD $Hf_{1-x}Zr_xO_2$ Deposited by Intermediate Annealing or Intermediate Plasma Treatment

M.N. Bhuyian[1], D. Misra[1], K. Tapily[2], R.D. Clark[2], S. Consiglio[2], C.S. Wajda[2], G. Nakamura[2], and G.J. Leusink[2]

[1]Department of Electrical and Computer Engineering, New Jersey Institute of Technology, Newark, NJ 07102, USA
[2]TEL Technology Center America, NanoFab 300 South, 255 Fuller Road, Suite 244, Albany, NY 12203, USA

Hafnium-based high-κ dielectric materials have been successfully used in the industry as a key replacement for SiO_2 based gate dielectrics in order to continue CMOS device scaling beyond the 22-nm technology node. Further scaling according to the device roadmap requires that highly reliable oxides with higher κ values be developed in order to scale the EOT to 0.7 nm or below. HfO_2 and ZrO_2 have similar chemical properties. Some reports have shown improved reliability for alloyed HfO_2 with ZrO_2 [1,2]. Recently, atomic layer deposited (ALD) HfO_2 and $Hf_{1-x}Zr_xO_2$ with a multiple deposition and annealing scheme was reported to be beneficial over a single post-deposition annealing by several groups [3-6]. However, the reliability of these films was not extensively studied.

In this work the reliability of atomic layer deposited $Hf_{1-x}Zr_xO_2$ with 80% Zr content has been analyzed in detail for three different oxide deposition processes. The ALD $Hf_{1-x}Zr_xO_2$ films were grown on an oxide interfacial layer (IL), grown chemically followed by nitridation (chemox+RFN). The deposition was carried out at 250°C by precisely controlling the Hf and Zr precursor pulses during the ALD cycles. One group of samples was subjected to dielectric deposition and thermal annealing in a cyclical process called DADA whereas the other group of samples was subjected to the same cyclical process with dielectric deposition and exposure to Ar plasma (denoted DSDS). The dielectric for the control samples was deposited without any intermediate step (As-Deposited). MOS capacitors (MOSCAP) were formed with TiN as a gate electrode material for electrical characterization.

Capacitance-voltage and current-voltage characteristics were evaluated before and after subjecting the MOSCAPs to a constant field stress of 2.75 × 10^7 V/cm in the gate injection mode. Flat-band voltage shift, ΔV_{FB} and stress induced leakage current (SILC) for different stress duration was monitored. The normalized flat-band voltage shift (Fig. 1) and SILC (Fig. 2) due to constant field stress at E=2.75 × 10^7 V/cm are plotted for DSDS, DADA and As-Deposited $Hf_{1-x}Zr_xO_2$ MOS capacitors. When subjected to constant voltage stress traps are generated in the gate dielectric and at the Si-IL interface. Below 100 s stress DSDS $Hf_{1-x}Zr_xO_2$ MOS capacitors showed reduced stress-induced trap generation and SILC whereas worse degradation was observed for DADA devices. With 1000 s stress, on the other hand, essentially identical degradation was observed in all devices.

Therefore, from our study, $Hf_{1-x}Zr_xO_2$ processed by DSDS seems to supress the oxide trap formation due to intermediate plasma exposure as it provides superior dielectric, EOT downscaling ability and good reliability performance. We will also compare the reliability characteristics of matching gate stacks with pure HfO_2 and outline the details of the contribution of interface states with various interfacial layers.

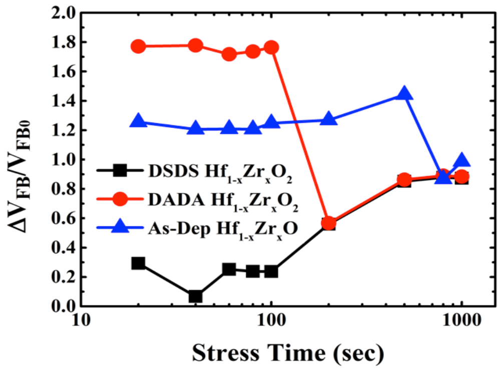

Fig. 1: Normalized flat-band voltage shift due to constant field stress at E=2.75 × 10^7 V/cm for DSDS, DADA and As-Deposited $Hf_{1-x}Zr_xO_2$ MOS capacitors

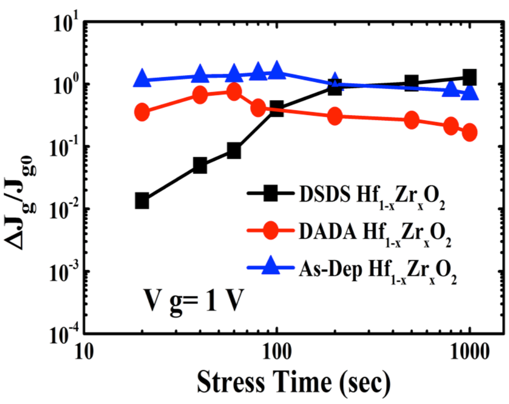

Fig. 2: Normalized stress induced leakage current due to constant field stress at E=2.75 × 10^7 V/cm for DSDS, DADA and As-Deposited $Hf_{1-x}Zr_xO_2$ MOS capacitors

References

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