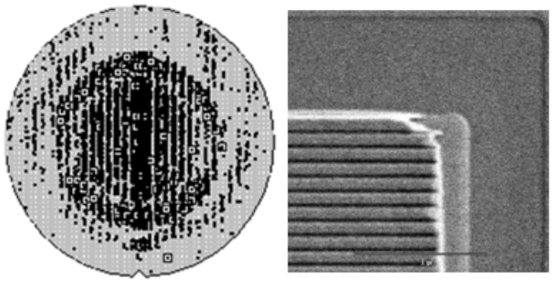
Characterization of the Descum Process for Various Silicon Substrates

C. Tiwari[1], Y. S. Lim[1], R. Fulton[1], J. Srinivasan[1], M. Gisinger[1], P. M. Flynn[2], L. H. Mak[2]
Micron Technology, Inc.
9600 Godwin Drive, Manassas, VA 20110[1]
8000 S. Federal Way, Boise, ID 83707[2]

The descum process is used to remove organic residue remaining after photolithography steps in the integrated circuit manufacturing process [1] [2] [3]. The descum process removes photo resist residue and provides a clean surface for subsequent process steps such as wet etch, implant, and dry etch [4].

Descum is a low-temperature, O_2-based plasma process with the objective of removing a few hundred angstroms of resist [5] [6]. This process is controlled by monitoring the resist loss on blanket wafers. Multiple process parameters have a major impact on resist loss, including process temperature, plasma power, and gas flow rates. These parameters are controlled by the manufacturing recipe and descum equipment settings.

In addition to recipe and equipment parameters, this paper demonstrates that the descum process is highly influenced by silicon substrate doping. The motivation for this study was the discovery that the descum process has a negative impact on wafer patterns. The descum process has removed more resist than was modeled in the manufacturing process flow, based on previous applications of the descum process. This exposed some unintended areas of the wafer to the subsequent dry etch process, damaging the wafer pattern (Fig. 1).



(a) (b)

Fig. 1. Negative effect of descum process shown by (a) wafer inspection map; (b) SEM image of damaged pattern.

Tests were conducted to understand and characterize the descum process. Fig. 2 shows the resist loss from a 44s descum process for two different types of silicon substrates. Type A wafers were lightly B-doped, while type-B wafers were highly B-doped. The resist loss for type-A wafers was ~400Å spread uniformly across the wafer, while resist loss for type-B wafers was ~5500Å at the center and ~1500Å at the edge.

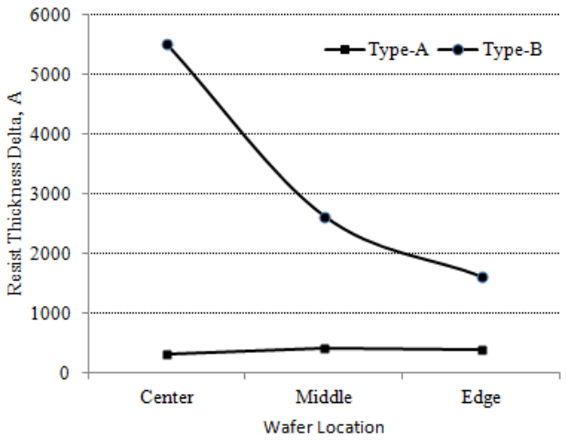


Fig. 2. Resist loss from descum process on two types of silicon wafers.

This paper presents a possible mechanism for the high resist loss and poor uniformity in type-B wafers, as well as the characterization of various factors.

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