Heteroepitaxial Growth of Sn-related Group-IV Materials on Si Platform for Microelectronic and Optoelectronic Applications: Challenges and Opportunities

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New materials such as Ge and group III-V compound semiconductor on Si platform has been developed in order to improve on the performance of metal-oxidesemiconductor field effect transistors (MOSFETs) and to add new functions of optoelectronic application. Snrelated group IV semiconductor alloy such as Ge_{1-x}Sn_x or $Ge_{1-x-y}Si_xSn_y$ is one of the most attractive materials for channels or stressors of MOSFETs. Tensile-strained Ge or Ge_{1-x}Sn_x has a potential which can realize high performance CMOS since they promise improving on carrier mobility of both electron and hole simultaneously. In addition, tensile-strain Ge with a magnitude of strain of 1% or $Ge_{1-x}Sn_x$ with a Sn content higher than 10% is expected to be direct transition semiconductor. That means optoelectronic device such as photo detector, light emitting diode (LED), and quantum well laser can be realized with only with group-IV materials on Si platform.

Considering application of Sn-related group-IV alloy materials, one of challenges is controlling Sn precipitation from Ge_{1-x}Sn_x or Ge_{1-x-y}Si_xSn_y alloy. The thermoequilibrium solid solubility of Sn in Ge and Si is lower than 1% in contrast to Si-Ge, complete solid solution system. Also, dislocations must be controlled to obtain optimum strain and energy band structures. In addition, point defects must be controlled in order to control concentration, mobility, and lifetime of carriers in films. However, influences of Sn incorporation, dislocation, and strains on the crystalline and electrical properties have not been understood yet compared to Si_{1-x}Ge_x system. We need to develop hetero epitaxial growth technology of Snrelated materials for application on Si platform [1,2].

Recently, we have achieved the heteroepitaxial growth of $Ge_{1-x}Sn_x$ layers with a very high Sn content of 27% [3]. Lowering the growth temperature and decreasing the strain induced lattice mismatch between $Ge_{1-x}Sn_x$ and substrate are essential key factors to suppress the Sn precipitation. We also found the optical energy bandgap can be decreased to 0.25 eV for a $Ge_{1-x}Sn_x$ layer with a Sn content of 27% which is grown on a InP substrate [4].

In order to enhance the carrier mobility, optimization of substrate orientation other than 001 is an attractive factor. Investigation of epitaxial growth of Ge and Ge₁. $_xSn_x$ on (110) or (111) substrate is required, although there are a few report compared to that related to a 001 substrate. Recently, we found that the Sn incorporation into an epitaxial Ge layer effectively suppresses the formation of twin defects [5-7]. Twin growth easily occurs in an Ge homoepitaxial layer grown on Ge(110) at a temperature as low as 200°C. On the other hand, we have achieved the growth of an 1.3%-Sn epitaxial Ge₁. $_xSn_x$ layers with no twin defect on Ge(110) at a growth temperature of 150°C. Also, the length of stacking faults in Ge_{1-x}Sn_x layers can be decrease to less than 10 nm with increasing in a Sn content from 1.3% to 4.6%.

Ternary alloy thin films of Sn-related group-IV semiconductor such as $Ge_{1-x-y}Si_xSn_y$ is attractive materials for multi junction solar cell, LED, and quantum well laser. Ge_{1-x-y}Si_xSn_y promises control of the energy band structure independent on the lattice constant. That realizes layer structure with multi-energy gap and no misfit strain. The compensation of local strain between Si and Sn atoms in Ge matrix effectively leads improving on the crystalline quality of Ge1-x-ySixSny layers and suppressing the Sn precipitation. The pseudomorphic growth of Ge_{1-x-} _vSi_xSn_v layers has been achieved even with a high Sn content of 15% (a Si content of 41%) and the Ge_{1-x} _vSi_xSn_v layer exhibits high crystalline quality [8]. No Sn precipitation occurs in a pseudomorphic Ge_{1-x-y}Si_xSn_y layer with a Sn content as high as 8% after the annealing 600°C, although the Sn precipitation occurs in a $Ge_{1-x}Sn_x$ layer with a low Sn content of 4.4% after the same annealing condition. Lowering the misfit strain between a Ge_{1-x-y}Si_xSn_y film and a Ge substrate is effective to increase in a Sn content much beyond the solubility limit and to stabilize Sn atoms at substitutional sites. We also confirm increasing in the energy band gap of Ge1-x-ySixSny layers with increasing in the Si and Sn contents to Ge one. Current-voltage characteristic of the undoped Ge_{1-x-} _vSi_xSn_y/n-Ge junction shows good rectifying properties, and the higher photo-response than the undoped Ge/n-Ge junction for the junctions at 1.0 eV can be observed.

The carrier behavior of Sn-related group-IV epitaxial layers is also investigated with Hall measurement [8]. Heteroepitaxial Ge_{1-x}Sn_x layers include a lot of point defects which generates holes. The hole concentration higher than 3×10^{17} cm⁻³ is observed in a Ge_{1-x}Sn_x layer grown on n-Ge substrate at room temperature. The Arrhenius plot of the hole concentrations indicates that there are three energy states which generate holes with different activation energies ranging from 2 meV to 90 meV. Especially, the density of the shallow energy state of 2 meV can be decreased with incorporation of 0.1%-Sn.

In summary, we can achieve the heteroepitaxial growth of $Ge_{1-x}Sn_x$ and $Ge_{1-x-y}Si_xSn_y$ with a very high Sn content taking advantage of non thermoequilibrium low temperature growth and considering the misfit strain and the compensation of local strain. We have to develop technologies for engineering the energy band structure and controlling the carrier behavior the heteroepitaxial layers. In future, we need to clarify the influence of Sn incorporation and strain structures on the defect formation and the carrier behaviors.

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References

- 1. S. Takeuchi *et al.*, Solid-State Electronics **60**, 53 (2011).
- 2. S. Zaima *et al.*, ECS Trans. **41**, 231 (2011).
- 3. M. Nakamura *et al.*, Thin Solid Films **520**, 3201 (2012).
- O. Nakatsuka *et al.*, Solid-State Electron. **83**, 82 (2013).
- Y. Shimura *et al.*, Appl. Phys. Express 5, 015501 (2011).
- 6. T. Asano *et al.*, Thin Solid Films **531**, 504 (2013).
- 7. T. Asano et al., Solid-State Electron. 83, 71 (2013).
- 8. T. Yamaha et al., ECS Trans. 50, 907 (2012).