3D Integration for an SOI Pixel Detector (Invited Talk)

Makoto Motoyoshi
Tohoku-MicroTec Co., Ltd. (T-Micro)
#203, 6-6-40 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan
Phone: +81-22-398-6264 E-mail: info@t-microtec.com

Abstract

Large-scale integration (LSI) technology in two dimensions has been the standard over the past three decades. However, the industry is now rapidly moving into the era of sub-20-nm nodes, and continuation of the present scaling trend will require the introduction of new transistors with three-dimensional (3D) structures and new materials and processes. This is expected to dramatically increase the development and manufacturing costs for systems on a chip. 3D-LSI is one solution that can mitigate the cost increases, without degrading the device performance. Consequently, many methods for realizing 3D-LSI devices have been developed by focusing on the unit processes of the 3D-LSI technology: (1) through-silicon via (TSV) formation, (2) bump formation, (3) wafer thinning, (4) chip/wafer alignment, and (5) chip/wafer bonding. However, these unit processes are incompatible in terms of various device and process requirements such as the process temperature, device structure, TSV and bump dimensions, yield, reliability, and supply chain. For bump connections, several reported methods are available, such as Cu–Cu bonding, intermetallic-compound bonding with Cu/Sn bumps, and Au bump bonding. Cu–Cu direct bonding can provide a good and robust connection but requires completely clean and flat surfaces. This would necessitate a dust-free environment, which is difficult to realize in practice for wafer/chip stacking with bump bonding. Although theoretically there might be many combinations of these five unit processes, they do not produce a device structure with good yield, reliability, and cost. This study investigated the optimal combination of unit processes for manufacturing an SOI stacked pixel detector chip for high-energy physics (Fig. 1). A pixel detector at the collider is designed to collect information about particles originating from the points where particles collide. In contrast to the image sensors of a digital camera, this device needs to detect fewer and much higher energy particles that pass through the device. The required key features of a pixel detector for this purpose are high sensitivity and high signal processing speed in order to increase space and time resolution. An SOI device provides both a high-sensitivity sensor area in the high-resistivity bulk substrate and a high-speed readout (RO) circuit area in the SOI. The incident charged particle generates a number of electron-hole pairs along its trajectory through the Si sensor. The generated holes are collected by the p+ diffusion layer in the high-resistivity Si substrate and sensed by the readout electronics circuits in the SOI layer. Stacking is accomplished with 2.5 μm × 2.5 μm In bump connections and adhesive injection at low temperature (less than 200°C). It is found that the stacking process is affected by the layout of each tier, adhesive injection is the key technology, and these effects could be minimized by optimizing the layout, process parameters, and device structure. Another concern for manufacturing the pixel detector is suppressing metal contamination. Some metals such as Au, Fe, and Pt form intermediate energy levels between the conduction and valence bands of Si and considerably lower the carrier lifetime. Cu is often used as a wiring and bump material in 3D devices. However, Cu diffuses into Si crystals and SiO_2 even at room temperature, increasing the leakage current of pn junctions and deteriorating the oxide quality of MOS transistors. For our 3D integration using In bumps, Au is used to protect In from oxidation. Considering these requirements, we have developed a 3D integration process for a pixel detector with a stacked SOI structure and In micro-bump (Fig.2).

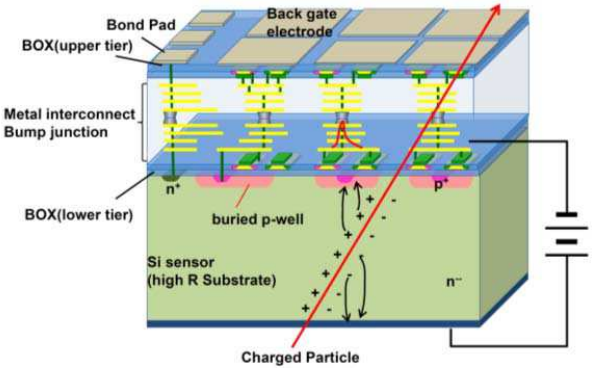

Fig.1 Stacked pixel detector

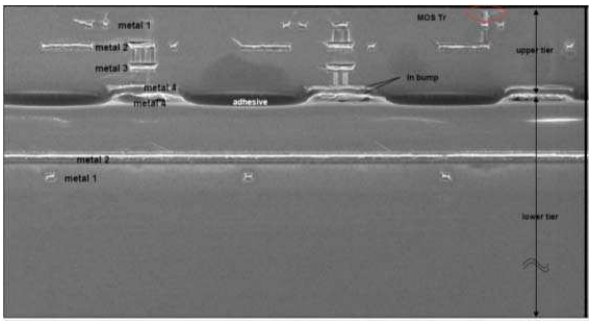

Fig.2 Cross-sectional SEM image of a stacked pixel detector