Using Graphene as a Conducting Layer for Through Silicon Via Filling

Shih-Cheng Chang and Wei-Ping Dow*

Department of Chemical Engineering, National Chung Hsing University, Taichung 40227, Taiwan

* dowwp@dragon.nchu.edu.tw

Graphene materials, including single layer and multi layer graphene platelet, have recently drawn extensive attention due to their outstanding electrical and thermal properties. Reduction of grapheme oxide (GO) is a method for preparaing the graphene film. Since GO has a large amount of oxygen functional groups, it can be well dispersed in several solvents and enable it to be coated on a substrate by a chemaical grafting method using a wet process[1].

Three-dimensional (3D) chip stacking is a major focus in recent research and development of microelectronics, MEMS, and MOEMS technology. Through silicon vias (TSV) play a key role in the 3D IC chip stacking connections. A main advantage of TSV is to make the shortest chip-to-chip vertical interconnection, which allows for size reduction of the chip and reducing signal transmission delay[2]. Electrodeposition plays an important role in TSV development, especially copper electrodeposition, which is a critical technology and generally used in the 3D chip packaging.

In TSV technology, the thermo-mechanical fatigue may lead to failure in the TSV interconnects[3] because the coefficient of thermal expansion (CTE) of copper is much higher than that of silicon. The package materials with different CTEs will induce large stresses at interfaces. In order to overcome this problem, we should choose tungsten to substitute copper. However, tungsten cannot be directly plated from an aqueous electrolytes, it can be co-deposited with iron group metals. Alternatively, since the CTE of graphene is closer to silicon than copper, we choose graphene sheets to substitute copper seed layer.

Traditional process for TSV fabrication is a dry process that includes the following step: (1) formation of vias by reactive ion etching; (2) formation of a SiO_2 isolation layer; (3) deposition of a TiN barrier layer and a copper seed layer; (4) electrodeposition of copper inside the via. In our research, we reduce the procedure of TSV fabrication using a wet process to substitute barrier and seed layer with graphene, and electrodeposition with Ni-W alloy to make a copper-free process. In other words, a copper-free TSV with simplified processing steps is fabricated, leading to lower fabrication cost. Moreover, a low-stress TSV filled with low CTE metals is also fabricated to improve the thermo-mechanical fatigue of TSV, leading to better package reliability.

References

1. P. Songfeng, and C. Hui-Ming, "The Reduction of Graphene oxide ", Carbon., 2012, 50, 3210-3228.

2. K. Kondo, T. Yonezawa, D. Mikami, T. Okubo, Y. Taguchi, K. Takahashi, and D. P. Barke, "High Aspect Ratio Copper Via Filling for Three-Dimensional Chip Stacking", J. Electrochem. Soc., 2005, 152, 658-662.

3. S. H. Choa, C. G. Song, and H. S. Lee, "Investigation of Durability of TSV Interconnect by Numerical Thermal Fatigue Analysis", Int. J. Pricis. Eng. Man., 2011, 12, 589-596.

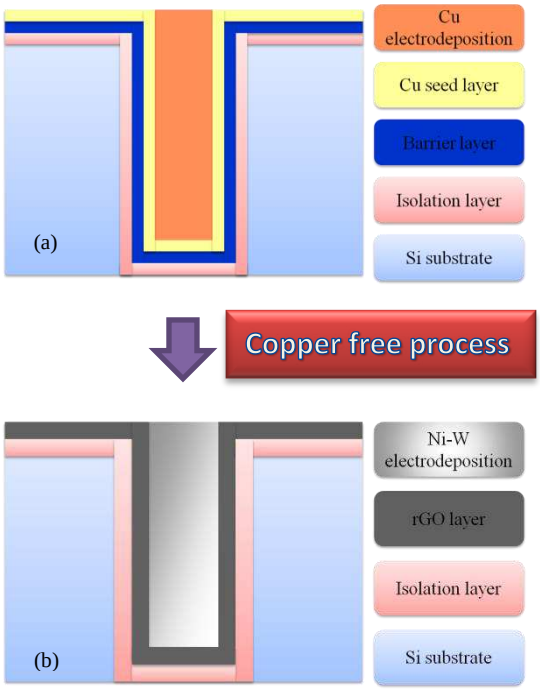

Figure 1. Schemes of TSV process (a) Traditional process and (b) Copper-free process.