

## Self-cleaning and Electrical characteristics of $\text{ZrO}_2$ ( $\text{HfO}_2$ )/GaAs (InGaAs) MOS capacitor fabricated by atomic layer deposition

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The reduction of native oxides on GaAs substrates is studied by predeposition cleaning as well as by short time pulsing of the metal precursor for self-cleaning mechanism using atomic layer deposition (ALD) of Trimethyl aluminum (TMA). The role of the predeposition cleaning followed by ALD application has significant effects in restraining the regrowth of native oxides. The short time pulsing of the TMA is effective for self-cleaning mechanism to reduce the intensity of GaAs native oxides. The reduction in native oxides on GaAs surface during ALD of TMA was investigated using X-ray photoelectron spectroscopy. X-ray photoelectron studies demonstrated that the pulsed deposition of TMA in the range of 2 to 4s is the most effective way of cleaning the GaAs native oxides. Our studies demonstrate a full proof self-cleaning process for GaAs wafers for any potential applications.

GaAs based metal oxide semiconductor (MOS) capacitors were fabricated with Zirconium Oxide ( $\text{ZrO}_2$ ) using ALD. The effect of growth temperature of  $\text{ZrO}_2$  dielectric films on GaAs was studied. The  $\text{ZrO}_2$  layers were deposited using Tetrakis Dimethyl Amido Zirconium (TDMAZr) and water in the temperature region 200 to 275°C. The as deposited samples have a significant amount of fixed charge in the bulk of the gate dielectric and at dielectric/semiconductor ( $\text{ZrO}_2$ /GaAs) interface, which causes the flat band shift and frequency dispersion. The post annealing in nitrogen ( $\text{N}_2$ ) reduces the flat band shift, frequency dispersion and capacitance-voltage (C-V) stretch out. In addition, the inversion characteristics of as fabricated capacitor were also improved with respect to the growth temperature and annealing. The gate dielectric stack is qualitatively illustrated through improved C-V characteristics and quantitatively verified by the reduced interface trap density ( $D_{it}$ ). The effect of  $\text{N}_2$  annealing is investigated in detail through electrical characterization and  $D_{it}$  measurements. We find that there exists a tradeoff where annealing improves C-V characteristics and reduces the  $D_{it}$ , however at the cost of higher leakage current. Similar studies will be presented for  $\text{HfO}_2$ .GaAs as well as InGaAs. The effects of interface traps as well as annealing temperatures on frequency dispersion will be discussed both experimentally and theoretically.

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