Abstract #2079, 224th ECS Meeting, © 2013 The Electrochemical Society

Investigation on Pad Surface Conditioner to Control Dishing Amount in Cu Damascene Process

Jong Won Kim[1], Hojoong Kim[1], SeokJi Hong[1], and HaSub Hwang[1]
[1]Memory Cleaning/CMP Technology Team, Semiconductor Business, Samsung Electronics, Hwasung, South Korea
E-mail: Jong.won.kim@samsung.com

Chemical mechanical polishing/planarization (CMP) process is a crucial process in semiconductor fabrication to construct highly ordered integrated circuit (IC) structure. In modern ultra large scale integration (ULSI) process, number of CMP process is remarkably increased to accommodate various materials and structures, such as metal interconnects and shallow trench isolation (STI).

In the CMP process, dynamic interaction of wafer and pad surfaces is a mechanism of material removal to prepare flat layer on wafer surface. During the interaction, chemical and mechanical effects are working at the same time to get the desired surface. Figure 1 shows configuration of CMP process. There are consumables of pad, slurry and conditioner. Each of them induces mechanical contact, chemical and abrasive reaction, and suitable pad surface topology, respectively.

For the construction of Cu interconnects, a CMP process called Cu damascene is needed due to its selective removal function between metal and oxide. Typically, 3-step polishing process is needed to get the damascene structure as shown in Fig. 2. In the step 1 and 2, bulk deposited Cu is removed with superior Cu/Oxide selectivity until barrier metal surface is exposed. Then, barrier metal, oxide, and Cu are removed by same removal rate in the step 3 to get high planarity.

Because, wafer is contacted with pad having elastic characteristic, pad asperity in contact might be deformed at pattern trench where Cu is filled. Furthermore, chemical in the slurry only reacts with Cu. Thus, there is a resulted phenomenon called ‘dishing’ as shown in Fig. 3. The amount of dishing represents resistivity of Cu line which influences performance of device directly. Thus, it should be controlled.

In our research, we tracked suitable pad surface to get optimal dishing amount for dynamic random access memory (DRAM) in 2x nm pattern pitch. The pad surface was modified by different types of CMP pad conditioner. From the experimental results, it was shown that dishing amount can be controlled by utilizing the conditioners in different design.

We prepared 5 types of the conditioner with different diamond pattern on their surface. The modification was intended to control dressing amount of pad surface between mild and aggressive dressing. Properties of the diamond pattern on the conditioner surface are listed in Table 1.

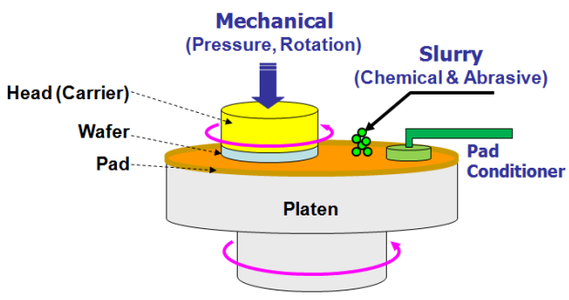

Fig. 1. Configuration and consumables of CMP process.

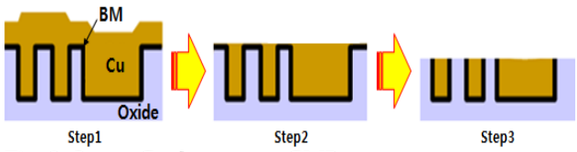

Fig. 2. 3-step Cu damascene CMP process.

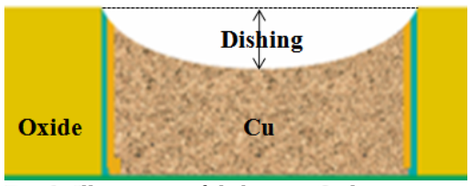

Fig. 3. Illustration of dishing in Cu line.

Table 1. Prepared pad conditioners for the experiment.

	Disk 1	Disk 2	Disk 3	Disk 4	Disk 5
Angle of diamond	Normal	Normal	Sharp	Normal	Sharp
Pattern Density	Low	Middle	Middle	High	High

From the polishing experiment with same slurry, and polisher condition but different conditioners, it was shown that surface topology of pad influences amount of dishing, vigorously. The used pads were analysed by various method such as contact area measurement, surface roughness measurement by 3D interferometer.

From the measurement results, we found that number of pad asperity which is contacted to wafer surface is highly correlated with removal rate as well as Cu dishing amount.

Finally, we tracked suitable contact condition between pad asperity and wafer. In conclusion, it was suggested that CMP pad conditioner with proper diamond pattern can control Cu dishing amount.