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Packaging Techniques for Compact SiC Power Modules Operable in an Extended Tj Range

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Because of their significant ability to operate with very low conduction and switching loss even at junction temperatures (Tj) of > 200°C, SiC unipolar power devices offer tremendous benefits for under-1.8 kV-blocking voltage-class power applications, including smaller size, lighter weight, greater robustness and superior cost effectiveness. Power modules aimed at these applications have been developed intensively worldwide in recent years. However, high Tj and greater thermal cycling cause them to deteriorate in a short period of time. Hence, one crucial concern is to ensure long-term reliability under severe thermal stress. This paper describes the packaging measures taken to address reliability challenges for the critical components--die attachment, wire bonding, encapsulation and insulating substrate--in direct contact with SiC devices inside the power module. Two preliminary numerical targets were set: (I) 3000 hours for a storage test at 250°C and (II) 3000 cycles for a thermal cycling test (TCT) between -40°C and 250°C. The test results showed that all of the components achieved these targets.

Die attachment—SiC die attachments formed with various Pb-free high-temperature solders consisting of AuGe, ZnAl, AuSn and BiAg were assessed in terms of joint strength reliability. The results obtained for AuGe die attachments are presented here. It was found that optimized AuGe die attachments could withstand 250°C storage for 3000 hours virtually without any decline in joint strength. In Fig. 1, (c) shows the results of a -40 to 250°C TCT for AuGe die attachments on a SiN substrate having a pair of Cu foils on both sides (denoted here as "Cu-SiN"). After 3000 cycles, the attachments barely fulfilled the joint strength criterion specified in IEC 67449-19. The steep decline in joint strength is a consequence of fatigue that developed in the solder layer due to cyclic stress caused by the large CTE mismatch between the SiC die (~5 ppm/°C) and the Cu foil (16.8 ppm/°C). In an effort to resolve this problem, the Cu foil on the substrate was replaced by a CIC (Cu/Invar/Cu clad) foil with a lower CTE (= 5.1 ppm/°C). As plotted in (a) and (b) in Fig. 1, excellent improvement was attained.

Wire bonding—Slightly Ni-doped Al wire of 200 μm in diameter was selected as the most adequate material at present. After soldering commercial SiC-SBD chips with AuGe onto Cu-SiN or CIC-SiN substrates, a pair of Al wires was ultrasonically wedge-bonded under optimal conditions so as to connect an Al pad (first bond) on the SBD to conductor foils (second bond) on the substrate. A 250°C storage test for 3000 hours revealed that the electrical resistance of the wires continued to monotonically decrease with increasing time while their bond strength dropped quickly in the early stage but then stayed at a level approximately two times higher than the criterion (70 gf) specified in IEC 60749-22. Figure 2 shows the results of a -40 to 250°C TCT conducted for wire samples on CIC-SiN. Pull strength declined with increasing cycles, albeit the rate of decrease lessened. After 3000 cycles, it was at a level of 127 gf, however, still satisfying the IEC criterion by a sufficient margin. On the other hand, the rise in electrical resistance stayed under 17%, which is acceptable, though not negligible.

Encapsulation—Silicone gel sealants (mostly prototype products) procured from four venders were comparatively tested periodically. At this time, one product has reached both the aforementioned storage and TCT targets.

Insulating substrate—A ceramic substrate is the only option available up to 250°C. In addition, the use of double-sided ceramic substrates with three conductive layers is preferable from the viewpoint of reducing parasitic inductance in the power module [1]. Double-sided ceramic substrates having a Cu/SiN/Cu/SiN/Cu structure were therefore fabricated and tested. It was found that the substrates showed superior durability in the 250°C storage test but failed within 1000 cycles in the 40°C to 250°C TCT. Failure was caused by delamination of the top and bottom Cu conductors, which was also caused by the big CTE mismatch between Cu and SiN (~3 ppm/°C). With the aim of resolving this problem, CIC/SiN/CIC/SiN/CIC substrates were prototyped and TCTs were conducted. The results demonstrated that the new double-sided ceramic substrates could withstand even a -40°C to 300°C TCT of 3000 cycles.

Acknowledgement

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Reference

[1] K. Matsui et al., Mater. Sci. Forum **717-720** (2011) 1233.

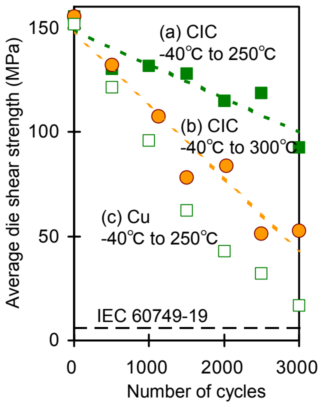

Fig. 1 Die shear strength of Au-Ge die attachment sample on (a), (b) CIC-SiN and (c) Cu-SiN as a function of the number of thermal cycles.

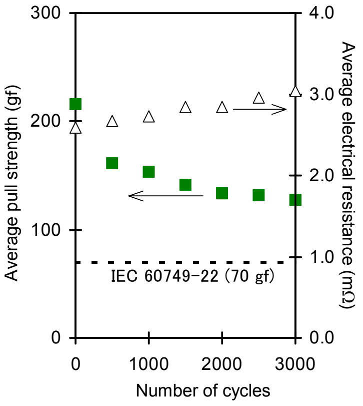

Fig. 2 Pull strength and electrical resistance of Al wire sample as a function of the number of -40°C to 250°C thermal cycles