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III-N High-Power Electronic Devices

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The III-N materials system offers a greatly increased power-switching performance and a dramatic theoretical advantage in the standard Figures of Merit for power electronic devices compared to Si- and other III-V- based power devices. III-N devices are also more suitable for operation in harsh environments because of their wider bandgap properties. These attractive properties of III-N materials have led to increased interest in their commercial application for “low-frequency” power switching applications. In addition, the III-Ns potentially offer a heterojunction bipolar transistor (HBT) technology with excellent high-power and high-speed performance for highly linear power amplifiers. Recent improvements in MOCVD epitaxial material growth and fabrication technologies have enabled a number of advances in the growth and fabrication of high-voltage heterojunction field-effect transistors (HFETs) on Si substrates, as well as the growth of GaN/InGaN *npn* HBT demonstrations that used a single-step epitaxial growth scheme. In this paper, we will present data on recent advances in both HFET-based high-voltage devices and on high-power III-N HBTs.

The limits of Si-based devices for solid-state power switches potentially can be greatly exceeded by GaN-based HFETs that feature high-current-drive, high switching-frequencies, and high-temperature-operation capabilities have sparked great interests for high-power switching applications in recent years [1-2]. Using GaN-based power transistors, it has been shown that high-performance power electronics can be realized to achieve low-energy-loss, compact, high-temperature, high-switching-speed, and hence high-efficiency systems. These features are important in the power electronic industries to overcome these challenges for next-generation solid state electronic switches that current Si-based power electronics are lacking [3-5].

The commonly used substrate for the implementation of GaN HFETs are SiC, GaN, or sapphire substrates [6-8]. In recent years, silicon substrates also have been extensively studied to exploit potential low-cost commercialization opportunities for power electronics due to good thermal conductivity and the availability for large-wafer sizes. Tremendous efforts have led to quite a few successful demonstrations of high-performance GaN HFETs on Si substrates. For examples, Hikita *et al.* developed a high power-power AlGaN/GaN HFET with a breakdown voltage of 350 V and a specific on-resistance of 1.9 mΩ-cm^2 by using a source-via grounding (SVG) design through 4 inch conductive Si substrate [9].

In this paper, we report depletion-mode 2.5-A AlGaN/GaN HFETs that have the specific on-resistance of ~6.2 mΩ-cm^2 and the blocking voltage of greater than 1.25 kV with the drain leakage current < 2.2 μA/mm. A study of the blocking voltage and the on-state resistance suggests that these switching figures of merit scale linearly with the gate-to-drain distance up to at least 2-kV for fabricated GaN-on-Si transistors.

We also report continued improvement of GaN-based *npn* double-heterojunction bipolar transistors (DHBTs) grown by metalorganic chemical vapor deposition (MOCVD) with state-of-the-art high collector current density (J_C) and low knee voltage (V_{knee}). For HBTs grown on sapphire, the common-emitter *I-V* characteristics show a high J_C ~19.8 kA/cm^2 and J_C = 28.6 kA/cm^2 from the Gummel plot with a offset voltage (V_{offset}) of < 0.22V and a V_{knee} < 2.1 V. The measured BV_{CEO} is 110 V. These values are among the best values reported to date for III-nitride (III-N) HBTs, suggesting that these DHBTs would be viable for high-power radio-frequency (RF) applications.

These results for GaN HBTs/sapphire show that high-performance III-N HBTs can be achieved without the need for complex re-growth schemes as reported earlier. To further develop III-N HBTs for RF power amplifications, high J_C, low V_{offset}, and low V_{knee} are required. In this talk, we will demonstrate that a large performance improvement can be obtained by the use of high-quality GaN substrates. Previously, the reported highest J_C for III-N HBTs was limited to ~10 kA/cm^2 [4], and V_{knee} were typically in the range of 5~15 V due to certain fabrication processing issues. In this study, the GaN/InGaN HBT fabrication process is further optimized through the low-resistive metallization and low-damage etching processing. As a result, dramatically enhanced J_C and lower V_{offset} and V_{knee} were achieved

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