A Study of Adopting Pure Tin Solder to Pillar Bump

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The conversion of solder bump electroplating material from leaded to lead-free; eutectic tin silver solder was widely adopted for lots of bumping application. But carrying out massive production using tin silver has several technical issues to overcome such as plate out(contamination) on the seal and silver ion stability in electrolyte. Because of these electroplate equipments have to be maintained mechanical manual scrubbing for every shifts and freshening bath periodically. In this study, we proposed binary to unary system as pure tin solder to get over wafer yield loss and environmental health and safety issue. Technical concerns of pure tin solder bump like tin whisker, tin pest issues, and increased melting point were considered and passed all of various massive torture tests.

World widely electrodeposited tin-silver solder material is used for bumping applications. Standard reduction potential for tin and silver is as following half cell reactions.

$Sn^{2+} + 2e^{-}$ → Sn : -0.138 V vs SHE (1)
$Ag^{+} + e^{-}$ → Ag : +0.799 V vs SHE (2)

Firstly higher silver redox potential makes hard to manage eutectic composition in bump deposits and simultaneously stabilization of silver ion together with within wafer composition uniformity. Secondly due to this large difference between tin and silver's reduction potential silver additive with stabilizer needs to be replenished frequently and this increase of chemical usage. And also we maintain equipment clean very often; every shift preventing seal plate out defect highly influenced by silver ion concentration which is not appropriate for high volume manufacturing. This study is dealing the root cause of seal plate out and proposing the solution for all the issues above.

When seal plate out defect occurs (Fig. 1(a)) bump height decreases leading to wafer yields drop (Fig. 1(b)). This mechanism was found to be that nucleation on seal defect sites due to disproportionation of silver ion or electron donation from tin(II) hereafter propagation and acceleration because of extreme edge dummy pattern border (Fig. 1(c)).

$3Ag^{+} \rightarrow 2Ag^{0} + Ag^{3+}$: disproportionation of Ag ion

$Sn^{2+} \rightarrow Sn^{4+}_{(\text{sludge formation})} + 2e^{-}$: tin oxidation
$Ag^{+} + e^{-} \rightarrow Ag$

Based on this hypothesis, we lowered silver concentration as tin-1.5silver and achieved seal plate out 70% decrease. And to find out specific extreme dummy pattern affect on seal plate out propagation and acceleration, photo shot map was modified to shoot only at particular intended spot (top) and rotated counter clock wise, plate out followed. From this result, we pushed forward to look upon pure tin electroplating bath and concerned risks to take

After reflowing electroplated pure tin solder bump, it makes solid solution with copper UBM (under bump material) as near eutectic tin-0.7copper solder. Formal studies from the literature[1,2] about tin copper solder already have reported better reliability and mechanical ductility than tin silver. Pure tin electrodeposits' IMC(inter metallic compound) layer is well defined as shown in Fig. 2(a). IMC grew flatter at both tin/copper and tin silver/copper interfaces (Fig. 2(a) and (c)). Internal solder cap, pure tin has smaller grains than tin silver after 750 cycling which is believed that this is due to resistance from Ag_3Sn particles. Furthermore ball shear test, oxidation, mounting torture test, tin whisker prevention, and reliability tests; preconditioning level 2, uHAST 500hr, TC 2000cycle, THB 600hr, HTS(180℃) 1000hr has all been qualified.

From this study we have confirmed that there will be no technical issues of using pure tin electrodeposits for bumping application. But it's still premature to adopt into massive production before fine tuning about wettability and compatibility on photo resist, throwing power and consume rate of additives.

Reference

[1] Hirokazu Ezawa, and et al., *2nd IEEE Electronics Systemintegration Technology Conference*, p719 (2008)
[2] Bob Sankman, *Future Directions for Flip Chip Interconnects, Semicon Japan STS Session 11 Packaging*, p6 (2013)

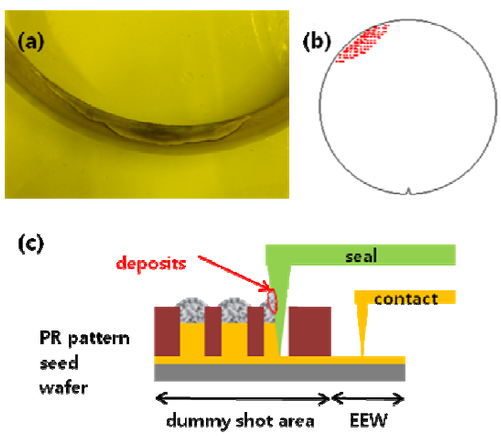

Figure 1. Image of plate out contamination on seal(a) with height yield map(b) and its predicted schematics(c)

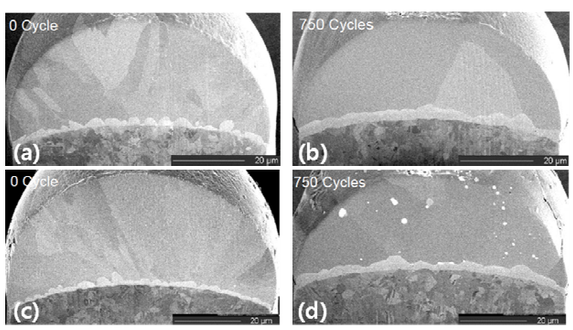

Figure 2. Comparison of IMC layer formation between pure Sn(a, b) and SnAg(c, d) solder before and after thermal cycling.