Storage Class Memory & NAND Flash Memory Hybrid Solid-State Drives (SSD)

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SSDs and emerging storage class non-volatile semiconductor memories (SCM) such as PCRAM, FeRAM, ReRAM and MRAM have enabled innovations in various nano-scale VLSI memory systems for personal computers, multimedia applications and enterprise servers. This paper provides a comprehensive review on state-of-the-art data management technologies of storage class memory and NAND flash memory hybrid solid-state drives (SSDs) [1, 2].

There is a growing demand for a high performance, highly reliable and low power SSD. A 3D TSV-integrated SSD with hybrid memory configuration which uses storage class memories (SCMs) and NAND flash memories is a promising solution. Among various SCMs, ReRAM is the best candidate due to its high speed, low power operation and potentially high scalability. In [1, 2], the detailed specifications for the ReRAM and architecture for the hybrid SSD are proposed as shown in Fig.1. The ReRAM uses NAND-like I/F. The polling (Ready/Busy status), which is used in NAND I/F, allows a variable access time. Three data management algorithms are proposed for the 3D hybrid SSD. The key idea is to store hot fragmented data less than the page size to ReRAM and use MLC NAND for sequential data. To evaluate the hybrid 3D hybrid NAND SSD a TLM (transaction level modeling) -based SSD emulator that can comprehensively simulate performance, energy consumption and P/E cycles has been developed.

Compared with the conventional MLC NAND SSD, the hybrid SSD shows 11 times higher performance and 79% lower write energy. By using 3D TSV interconnects, the I/O energy is reduced by 27 times because the huge capacitance of the wire bonding is almost eliminated. As a result, the total SSD energy reduction reaches 93%.

Furthermore, the slope of the average MLC NAND P/E cycles is decreased by 6.9 times by the hybrid SSD. This directly corresponds to a reduction in the replacement cost of a SSD storage system because the slope determines the aging speed of the SSD.

In ReRAM, a data fragmentation does not occur because the partial overwrite is possible. As a result, the slope of the ReRAM P/E cycles is limited to 28 times of that of the MLC NAND in the hybrid SSD. Assuming MLC NAND endurance of 3×103, the required P/E cycles for ReRAM is less than 105, which is acceptable for the ReRAM device characteristics. The valid pages are scattered in the conventional SSD indicating that frequent overwrites have occurred to the MLC NAND.

On the other hand, the hybrid SSD efficiently uses ReRAM and shows less fragmentation of MLC NAND because overwrites to MLC NAND are suppressed.

The required ReRAM latency to obtain sufficient improvements is also investigated. ReRAM read latency is also varied. From the figures, both ReRAM write and read latency should be less than 3us to maintain high performance and low power operation. Considering 50ns write pulse, the 3us access is achievable for ReRAM in write verify operation.

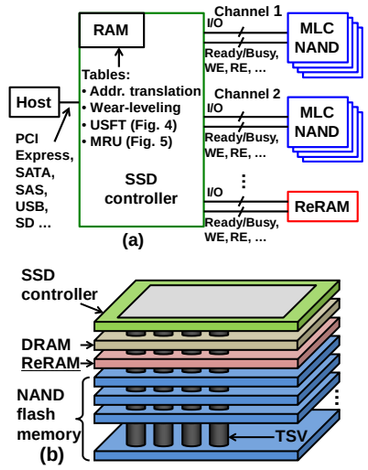

Fig. 1 (a) Block diagram of the proposed 3D TSV-integrated hybrid ReRAM/MLC NAND SSD. Proposed ReRAM uses NAND-like I/F. (b) Physical image of the proposed SSD.

References

[1] H. Fujii et al., *Symp. VLSI Circuit*, pp. 134-135, 2012.
[2] K. Takeuchi, *Inside Solid State Drives*, Chapter 7,13, 2012.