3D Integration and Reliability Challenges

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Introduction

3D LSIs using TSVs are indispensable to achieve high performance and low power LSIs with smaller form factor [1]-[3]. To fabricate 3D LSI, each functional wafer should be thinned to 10-50μm thickness. However, the ultra-thin nature of Si substrate leads to several problems such as weak mechanical strength, warping, local deformation, and residual stress in the stacked die. In addition, the large CTE difference between Si substrate and Cu TSV and μ−bump is posing risks of undesired thermo-mechanical stress generation and Cu contamination in the active Si of thin LSIs. In this paper, we focus our attention on some of the most potent reliability issues such as thermo-mechanical stress, crystal defects, and Cu contamination introduced in 3D integration processes.

Wafer thinning and Crystal defect

The residual stress and sub-surface defects present in the ultrathin wafer stress-relieved by CMP (chemical mechanical polishing), PE (plasma etching), UPG (ultra-poly grinding), PG (poly grinding), DP (dry polishing), and #2000 after back-grinding are evaluated [4]. The 2D-stress mapping data obtained on the stress relieved surface of ultra thin wafers with 10 μm thickness revealed that the active surface of the wafers is under severe tensile stress of +35 to +40 MPa. Among various stress relieved wafers examined for the residual stress at the back-ground surface after wafer thinning, the μ-Raman data revealed that there exists a compressive stress of -30 MPa and -75 MPa respectively for 50 μm thick DP and CMP samples; whereas in the case of 10 μm thick wafers, regardless of the stress relief process, both the CMP and DP wafers possessed around -100 MPa of tensile stress. As formed sub-surface defects in the DP-stress relieved wafers could well act as an external getter sites for the heavy metal atoms originating from the backside metal contaminants.

Mechanical stress by TSV and microbumps

We have evaluated mechanical stresses induced by Cu-TSV using the micro-Raman spectroscopy (μRS) [5]. The mechanical stress profiles measured along the horizontal direction for square Cu-TSVs with 10μm-width and 20μm-pitch at various annealing temperatures indicated that the pure tensile stress not accompanied by the compressive stress was observed in the Si substrate between Cu-TSVs when the annealing temperature was lower than 200 ℃. This tensile stress changed to the pure compressive stress not accompanied by the tensile stress when annealed at the temperature higher than 200 ℃. Thus compressive stress significantly increases at the center of TSV array. This increased pure compressive stress causes not only serious die cracking but also Cu extrusion (pop-up) and Cu peeling.

The local mechanical stress is also generated by the local deformation around μ-bump region. It is worthy to note that the magnitude of locally induced mechanical stress and its propagation along the plane of the active Si due to local bending was too high as compared to the thermo-mechanical stress induced by the metal-TSVs and μ−bumps. For example, the μ-bump array (where the bump size and bump spacing of 5μm and 100μm respectively) introduces a maximum tensile stress of more than +1500 MPa in the active area of top die around the μ−bump region. Such a large tensile around the μ−bump region not only deteriorates the device performance, but also severely degrades the mechanical strength of the stacked die, which results into the die-crack.

Cu diffusion from the backside and TSV

The Cu diffusion behavior from the backside and Cu-TSV was evaluated by the C-t method using the planar MOS capacitor and the trench MOS capacitor with Cu/Ta gate electrode. It was confirmed that C-t curves seriously degraded by intentional Cu contamination from the backside in thinned wafers when any gettering regions were not formed. In the evaluation of Cu contamination from TSVs, two types of the sidewall scalloping with average roughness of 30 and 200 nm were prepared by the Bosch process to compare the influence of the step coverage of barrier layer [6]. After the formation of a 100-nm-thick oxide liner into via holes, Ta barrier layers with thicknesses of 10 and 100nm (at the surface) were formed by sputtering. The thicknesses of sputtered Ta layers at the sidewall of TSV are approximately 3 (10 nm at the surface) and 20 nm (100 nm at the surface), respectively. The C−t curves of the trench capacitors with 10nm thick Ta layer (at the surface) show a severe degradation after the initial annealing for 5 min. It was revealed that the generation lifetime derived from the C-t curve rapidly decreases as the distance from the TSV decreases. This indicates that Cu atoms diffuse into the active area from the Cu TSV through scallop portions with extremely thin Ta layer in TSVs.

Degradation of DRAM retention by wafer thinning and Cu contamination

The control of the retention time (refresh) for the stored charge is a key issue for realizing reliable 3D-DRAM. Possible origins for the degradation of retention characteristics in 3D-DRAM are crystal defects and Cu contamination. Then the influences of crystal defects introduced in Si thinning process and Cu contamination from the backside surface on DRAM retention time were electrically characterized [7]. As a result, it was revealed that the DRAM retention characteristics were significantly degraded by the change of crystallinity and mechanical stress caused by Si thinning as the Si substrate thickness decreased below 30μm, and by Cu contamination as the Cu is intentionally diffused from the backside surface for 30 min at 300 ◦C.

Conclusion

We revealed that the stress relieved surface of ultra thin wafers with 10 μm thickness was under severe tensile stress It was found that the mechanical stress locally induced around μ−bumps after stacking dies was very high as compared to the thermo-mechanical stress induced by the metal-TSVs and μ−bumps. We revealed that the generation lifetime significantly decreased by the Cu contamination from the backside and TSVs and confirmed that the DRAM retention characteristics were degraded by thinning the Si substrate and the Cu contamination from the backside.

References

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