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Impact of STI gap-fill process deposited by HDP-CVD in flash memory

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The effects of shallow trench isolation (STI) gap-filling process deposited by high density plasma chemical vapor deposition (HDP-CVD) were investigated by comparing with TEOS+O_3 undoped silicate glass (USG) process in NAND flash memory. HDP CVD oxide has been widely used for STI process because of its excellent gap-filling capability in relatively low temperature. However, it is well known that HDP-CVD process has problems caused by plasma-induced damage (PID) [1]. Thus thin thermal oxide was introduced as a buffer layer in order to minimize the plasma charging effect. In addition, there is also hydrogen related problem which is dissociated from SiH_4 precursor in plasma. Hydrogen has both beneficial and deleterious effect to the gate integration [2].

The comparative sub-threshold swing degradation of the cell after F-N current stress of 0.13C/cm^2 [3] is shown in Fig. 1. Initial swing is almost the same which indicates that PID during process is not dominant since the direct plasma damage was shielded by buffer oxide under layer. However, after stress, the swing of HDP-CVD gap-filled device is 20% more degraded than USG. The calculated interface state density (D_{it}) of the HDP-CVD is also 23% more than USG. It is insufficient to explain only with PID model. It was reported that hydrogen ions in plasma penetrate into underlying thermal oxide and they are drifted into the Si substrate by high electric field [4]. Although TEOS+O_3 USG process also contains hydrogen species in precursor, the hydrogen atoms or ions have little kinetic energy to penetrate into underlying layers since there is no applied electric field or RF bias. Fig. 2. shows the hydrogen contents in both devices confirmed by thermal desorption spectroscopy (TDS) spectra after field recess process. HDP-CVD gap-filled device contains 50% more hydrogen concentration. It is well known that the role of atomic hydrogen is passivation of the Si dangling bonds in the Si/SiO_2 interface (Si· + H_2 → Si-H + H_0) during the forming gas annealing (FGA) process. Simultaneously, the atomic hydrogen also depassivate the Si-H bonding (Si-H + H_0 → Si· + H_2) at room temperature [5,6]. As a results interface trap generation by atomic hydrogen depends on the ratio of passivation and depassivation. The HDP-CVD gap-filled device contains a large amount of hydrogen as we measured, and they can easily diffuse to tunnel oxide and degrade the cell transistors in flash memory. Fig. 3. shows average V_{th} shift of 64M cell array according to P/E cycling stress. The v_{th} of HDP-CVD gap-filled device shifted 15% more than USG due to the oxide trap and interface trap generation by F-N current stress [7]. It is consistent with the swing degradation and the hydrogen depassivation model. We have demonstrated the effect of the plasma-deposited HDP-CVD STI gap-fill process which contains hydrogen species in the precursor and confirmed the degradation mechanism of the cell in flash memory.

References

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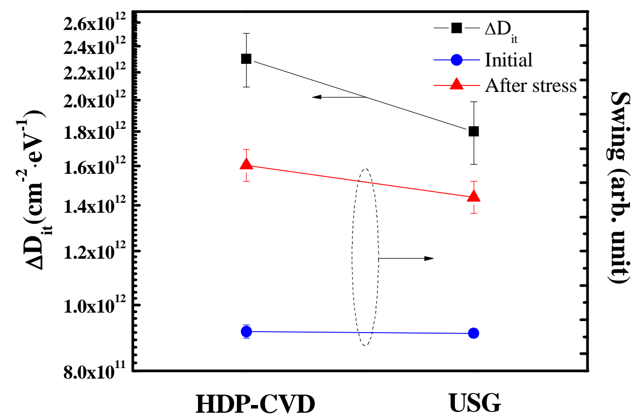

Fig. 1. Swing shift after F-N current stress of 0.13C/cm^2 and calculated the change of interface state density.

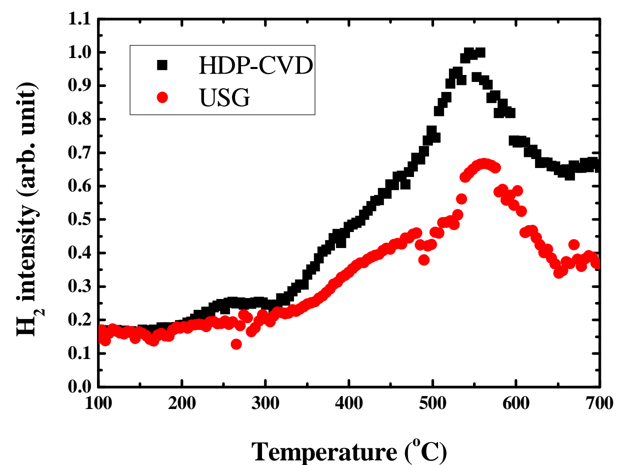

Fig. 2. TDS spectra of hydrogen desorption after field recess process.

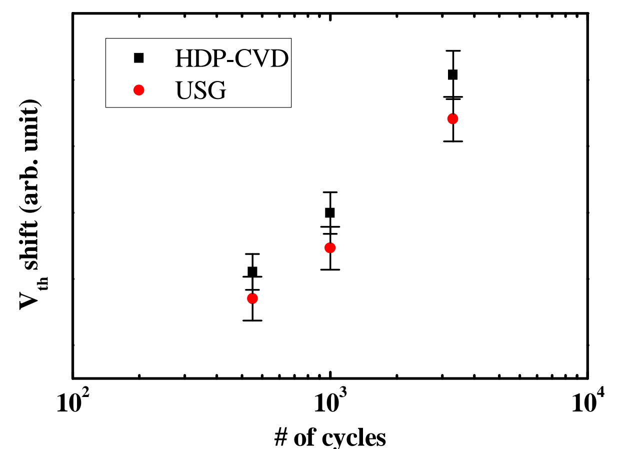

Fig. 3. V_{th} shift of cell array during P/E cycling stress.