Evaluation of TaN as the wet etch stop layer during the 22nm HKMG gate last CMOS integrations

Hushan Cui, Jing Xu, Jianfeng Gao, Jinjuan Xiang, Yihong Lu, Zhaoyun Tang, Xiaobin He, Tingting Li, Jun Luo, Xiaolei Wang, Bo Tang, Jiahan Yu, Tao Yang, Jiang Yan, Junfeng Li and Chao Zhao

Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, 100029, China

The recent development of high-k/metal gate (HKMG) is the major trend of device scaling as to continue the Moore's law [1]. In order to implement nMOS and pMOS simultaneously, an etch process is compulsory to remove TiN & Ti work function metals of pMOS covering nMOS region selectively, as shown in Fig. 1 [2]. Though both dry and wet etch work, dry etch approach may not be a good way in view of possible plasma damage on underlying high-k and/or its cap layer [2, 3]. Wet etch approach, therefore, is preferable to be adopted. Such an approach necessitates the insertion of a wet etch stop layer (WESL), typically TaN between nMOS and pMOS work function metals because of potential good selectivity of TiN towards TaN [3]. In this work, TaN WESLs deposited by two different methods, *e.g.*, PVD and ALD, are evaluated and their effect on work function of metal gate is studied using C-V method with MOS-capacitor (MOSCAP).

The wet etch rates of ALD and PVD TaN films on blank wafers in ammonia peroxide mixture (APM) solution were checked [3, 4]. Thicknesses of TaN were determined by Spectroscopic Ellipsometry (SE) and Four-Point Probe (4PP) as well as Scanning Electron Microscopy (SEM). For p-type MOSCAP (nMOS), after wet etch to strip TiN & Ti of n-type MOSCAP (pMOS) as shown in Fig.1, TiAl work function metal was sputtering-deposited. C-V characteristics of both n- and p-type MOSCAP on the same wafer were measured.

In Fig. 2, for PVD TaN films with different nitrogen content (tuned by N_2 flow rate), the evolution of resistivity with APM process time is shown. Two observations can be made. First, the resistivity of TaN films increases as the increase of nitrogen content. Second, at low nitrogen content (N_2 flow rate $\leq$ 3 sccm), TaN films are quite resist to APM etch since the resistivity remains almost unaltered with process time. However, at high nitrogen content (N_2 flow rate $\geq$ 5 sccm), the PVD TaN films becomes less chemical resist to APM etch which is in line with results in [3, 5]. ALD TaN shows much better chemical resistance to APM (results not shown). Nevertheless, for TiN/Ti/TaN stacks, no matter ALD or PVD TaN would be gently attacked by APM solution. It may be due to an easily attacked interfacial layer by APM created by Ti diffusion into TaN [6].

The C-V characteristic of n-type MOSCAP (pMOS) and p-type MOSCAP (nMOS) are shown in Fig. 3 and Fig. 4 respectively. It can be seen that ALD TaN has negligible impact on V_{FB} for n-type MOSCAP (Fig. 3), indicating that ALD TaN works well not only as a WESL but also a work function tuning layer. However, the thickness of ALD TaN greatly impacts V_{FB} of p-type MOSCAP (Fig. 4), since V_{FB} shifts to more positive value as the increase of ALD TaN thickness. It can be anticipated that thick ALD TaN prevents TiAl from reaching high-k thus fail to tune the nMOS work function.

In conclusion, both PVD and ALD TaN can be used as WESL. For both n- and p-type MOSCAP, PVD and ALD TaN can be used as WESLs, but only if the thickness of ALD TaN cannot exceed 1 nm for p-type MOSCAP otherwise TiAl as work function metal cannot penetrate it thus fail to tune work function. Considering the excellent filling capability of ALD TaN, it will be extensively used in advanced CMOS technology as WESL.

References

[1] A. Veloso *et al.*, VLSI (2011).
[2] S. B. Samavedam *et al.*, IEDM (2002).
[3] M. M. Hussain, N. Moumen, J. Barnett, J. Saulters, D. Baker and Z. B. Zhang, Electrochem. Solid-State Lett. **8**, G333 (2005).
[4] R. Vos, S. Arnauts, I. Bovie, B. Onsia, S. Garaud, K. D. Xu, H. Y. Yu, S. Kubicek, E. Rohr, T. Schram, A. Veloso, T. Conard, L. H. A. Leunissen and P. Mertens, ECS Trans. **11**, 275(2007).
[5] C. S. Kang, H. J. Cho, Y. H. Kim, R. Choi, K. Onishi, A. Shahriar and J. C. Lee, J. Vac. Sci. Technol. B **21**, 2026 (2003).
[6] Z. B. Zhang, S. C. Song, K. Choi, J. H. Sim, P. Majhi, B. H. Lee, Device Research Conference Digest(2005).

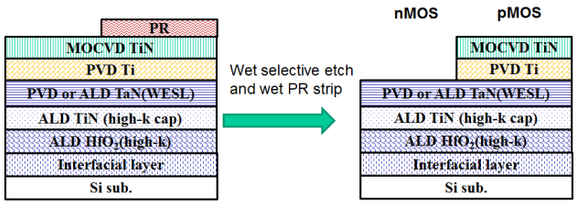

Fig. 1 A wet selective etch was implemented to remove pMOS work function metals, TiN & Ti, selectively from the nMOS region.

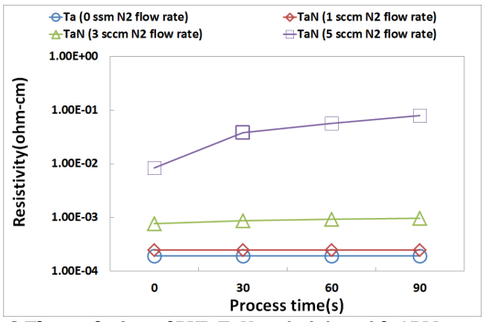

Fig. 2 The evolution of PVD TaN resistivity with APM process time

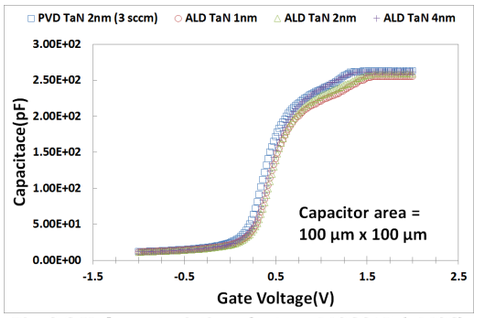

Fig. 3 C-V characteristics of n-type MOSCAP (pMOS)

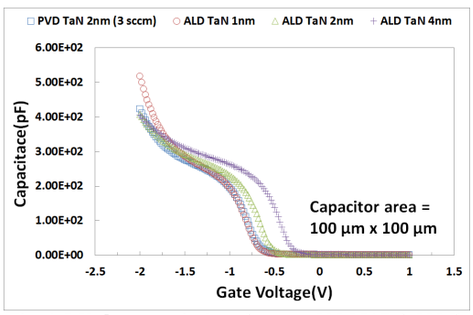

Fig. 4 C-V characteristics of p-type MOSCAP (nMOS)