Properties of Al-SiO_2-SiC(3C) structures with thermally grown and PECVD deposited SiO_2 layers

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MOS capacitors on two wafers of SiC(3C) substrates were characterized. Crucial parameters of structures on both wafers are measured and compared.

Samples: MOS capacitors were fabricated by Acreo on two 3" n-type 3C-SiC (001) wafers. The wafers consisted of ca. 200 µm thick substrates from Hoya with doping of $5*10^{18}$ cm^{-3} and an n-type epilayer with 12 µm thickness and nitrogen doping of $7*10^{15}$ cm^{-3} grown at Acreo. Wet thermal oxide was grown at 1150 ºC for 1 hour on the first wafer and the PECVD oxide was deposited at 300ºC on the second, both to a thickness of ca. 60 nm. The second wafer was further annealed at 950C for 3 hours in wet oxygen [1,2]. Both wafers were divided in quarters and MOS capacitors were fabricated by forming circular Al, Ni, and Au metal gates of 0.7, 0.6, 0.5, 0.4 and 0.3 mm diameter and with different thicknesses: t_{Al} = 25, t_{Ni} = 10, t_{Au} = 15 nm using ion beam sputtering and lift-off.

SiO_2 breakdown voltages: Leakage currents and breakdown voltages were measured for at least 12 structures on each wafer. Taking arbitrarily the current density $J=10^{-6}$ A/cm^2 as the breakdown condition, the average breakdown voltages V_{BR} were determined for structures on both wafers. A histogram of V_{BR} measurement results is shown in Fig.1. Notice the significant difference in V_{BR} values. For structures with thermal oxides 79% of devices broke down below 40 V, while for structures with PECVD oxides it was only 64%.

Trap distributions: Using the conductance method energy distributions of traps were determined for structures on both wafers. Averaged results are shown in Fig.2, showing that the density of deeper lying traps is lower for structures with thermally grown SiO_2.

Band diagrams: Using photoelectric and electrical measurement methods [3,4] complete band diagrams of capacitors on both wafers were determined. The general representation of band diagrams for the state of flat-band in the semiconductor (ϕ_S=0) and of flat-band in the dielectric (V_{ox}=0) is shown in Fig.3. The values of all the potentials in the figure are given in Table 1, for structures on both wafers.

Raman spectra. An example of spectra taken for both samples with MonoVista 2750i micro-Raman spectrometer using 266 nm UV excitation laser line is shown in Fig.4.

Conclusions. Noticeable differences were found in breakdown voltages (Fig.1) and trap distributions (Fig.2) of structures on wafers no.1 and 2. Breakdown voltage is slightly higher for PECVD deposited SiO_2 layer, while the density of traps is lower for structures with thermally grown SiO_2 layer. No significant differences were found in the band diagrams and Raman spectra of structures on both wafers. The latter means that there are no significant differences in mechanical stresses in structures of both kinds. Use of deposited and densified oxide improves the gate breakdown and allows to reduce the thermal budget of the MOSFET processing

References.

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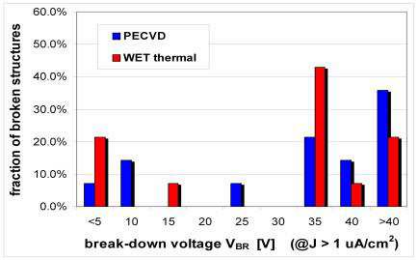

Fig. 1. Histogram of breakdown voltages

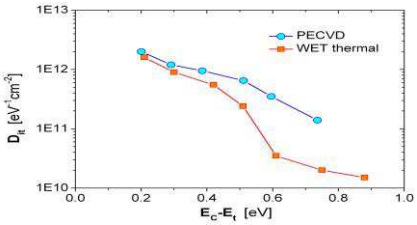

Fig. 2. Density of traps vs. depth in the band-gap

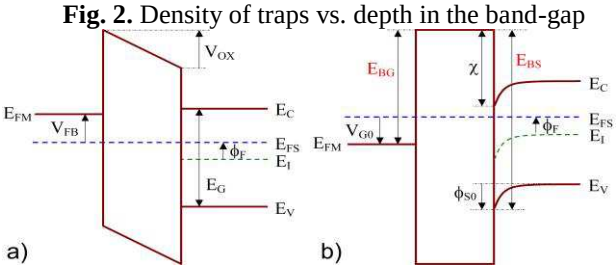

Fig. 3. Band diagram at two gate voltages V_{FB} and V_{G0}

Table 1. Values of potentials shown in Fig.3.

Oxide	E_{BG} [eV]	E_{BS} [eV]	χ [eV]	ϕ_F [V]	ϕ_{MS} [V]	V_{FB} [V]
PECVD	3.425	5.455	3.094	-0.961	0.028	-1.196
WET thermal	3.466	5.897	3.536	-0.981	-0.038	-0.914
Oxide	**Q_{eff} [C/cm²]**	**N_{eff} [cm²]**	**ϕ_{S0} [V]**	**V_{G0} [V]**	**V_{OX} ($V_G = V_{FB}$) [V]**	
PECVD	$7.14 \cdot 10^{-8}$	$4.46 \cdot 10^{11}$	0.097	0.126	-1.225	
WET thermal	$5.42 \cdot 10^{-8}$	$3.38 \cdot 10^{11}$	0.082	0.044	-0.877	

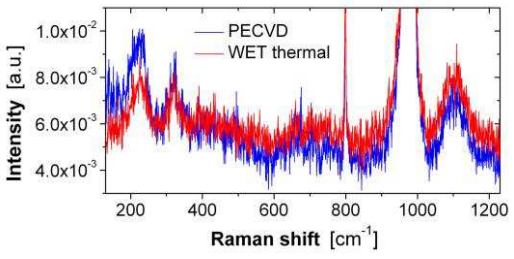

Fig. 4. Raman spectra of both types of SiO_2 layers