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# Reliability Challenges of 3-D stacked chip package with Through-Silicon-Via

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**Abstract**

3-D stacked chip package, using TSVs (Through Si Via), has drawn considerable interest in the semiconductor industry, because TSV technology can provide lower power consumption requirements, higher bandwidth, and smaller form factors. However, there are lots of reliability issues in the development stage. And we should clear away them before mass production of 3-D stacked chip package.

In 3-D TSV stacked chip structures, not only TSV but also micro-bumps and inter-chip gap filling adhesives are implemented. So, compared with conventional package (wire bonded package), 3-D stacked chip packages, using TSVs, contain three major different structure and process. First thing is TSV itself, second thing is both-side micro-bumps for solder joining, and last thing is wafer backside process which silicon surface is revealed prior to back side bump formation. These different things make various reliability issues. But, up to now, there have been few studies how new structures and processes have influence on the reliabilities in overall points of view for the 3-D TSV integration.

In this paper, an overview of reliability issues of 3-D stacked chip package is introduced dividing into three categories: zero-level reliability of FEOL (front-end of the-line) such as transistors and capacitors, 1$^{st}$ level of BEOL (back-end of the-line) metallization and TSV interconnections, and 2$^{nd}$ level of micro-bumps of stacked chip interfaces.

This paper describes the essential scope of the reliability challenges in 3-D IC packaging technology by dealing with reliability issues from transistor-level of the memory device to package micro-bump level of chip-to-chip interconnections and material effects on each level's reliability issues.