Characterization and performance of D-mode GaN HEMT transistor used in a cascode configuration

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GaN as a material system has been the subject of intensive research over the last 20 years. The initial demonstration of this material system was focused on light emitting structures as a potential source of compact blue/UV LED solid state emitters. The first single crystal GaN transistor was demonstrated in 1993 by Khan et al[1]. This was quickly followed by the demonstration of an AlGaN/GaN HEMT device also by Khan[2] et al in 1993. Over the years, the quality of the material from advancements in growth deposition techniques and device processing has steadily improved. Now, GaN HEMT devices are on the brink of becoming practical for use in the high-voltage power switching arena.

GaN Systems is developing a depletion mode high voltage high current AlGaN/GaN HEMT (D-HEMT) device integrated in a cascode configuration. The D-HEMT device is fabricated on a SiC substrate with a typical gold lift off process. The device has exhibited excellent low field 2DEG mobilities greater than 1500 cm^2/V-s and saturation currents of 590mA/mm at room temperature. The average breakdown field strength under oil was as high as 90 V/μm of Lgd. It reduced as Lgd was increased beyond 12μm. This reduction was attributed to surface related effects that started to dominate the breakdown process. The breakdown voltage and DC on-resistance of the large GaN D-HEMT device used in the cascode configuration has been measured to be >600 volts and 150mΩ respectively. The custom NMOS device used in the cascode was fabricated with a 0.8μm CMOS technology and has an on-resistance of 15mΩ. Also included on the CMOS die is a custom integrated differential input with Schmitt Triggers, driver and slew rate control circuits, to add to the overall functionality and ease of use of the cascode configuration.

Designing high-voltage, high-current switching devices requires close attention to reducing parasitic capacitance and the resulting displacement currents that flow during switching. A significant source of the parasitic capacitance arises from the presence of field plates. Field plates are used to control the peak electric field within the 2DEG channel to increase the breakdown voltage[3] and reduce the effects of dynamic on resistance[4]. The design and configuration of the field plates will influence the device output capacitance Coss. For a cascode connected device, control of the HEMT source and NMOS drain common node is particularly important. How the field plates on the GaN device are connected will have an influence on the maximum common node voltage during switching. This voltage will place additional requirements on both the GaN device Schottky gate, as well as the breakdown voltage of the NMOS device.

To increase the current density efficacy and reduce parasitic inductances on chip, copper posts have been used to move the current vertically off the GaN device, allowing it to be flipped onto the top of the NMOS transistor. The whole assembly has been placed into a custom 10mmx10mm PQFN package.
Extensive 3D thermal-electrical modeling has been used to optimize the thermal aspects of this assembly. It has been determined that the total thermal resistance of the PQFN package is less than 2.5°C/W.

The packaged device, in a hard switching circuit, has demonstrated 500 volt operation with load currents of 5 amps. In addition, resistive switching voltage slew rates have been measured as high as 72V/ns. The beneficial use of slew rate control has also been successfully demonstrated for optimizing the GaN HEMT cascode performance.

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