Effects of Sulfur Passivation on Ge/GeSn MOS Capacitors with HfO_2 Gate Dielectric

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To improve CMOS device performance, extensive research on high mobility materials has been done. Recently, GeSn alloys having higher hole mobility than Ge was demonstrated to be a possible channal material [1]. A GeSn pMOSFET has been realized and exhibits a higher hole mobility compared to that of Ge control pMOSFETs [2]. However, similarly to Ge, proper passivation of the GeSn/HfO_2 interface is one of the most challenging issues to be resolved before it can be used as a channel material. Sulfur Passivation of Ge surfaces by immersing the wafer into $(NH4)_2S$ solution prior to high-k film is one passivation solution for Ge surface because it leads to improved performance of Ge-based devices [3]. Thus, in the paper, firstly we implement an ultrathin GeSn layer on Ge surface by first sputtering Sn on the Ge substrate and then removing the top Sn layer with diluted HCl solution. Then the effect of sulfur treatment of GeSn/HfO_2 interface by the $(NH4)_2S$ solution method was investigated in this study.

The starting wafers for the experiment were (100) oriented n-type Ge wafers. After cyclic rinsing between deionized water and diluted HF, a Sn layer(~35nm) was deposited on Ge substrates using a magnetron sputtering system, and after 200˚C, 30min RTA, the top Sn layer was removed using diluted HCl solution, leaving an approximately 1-nm-thick GeSn layer. After that, the substrates were immersed into 20% aqueous $(NH4)_2S$ solution for 30 min at room temperature. 5.5-nm-thick HfO_2 was deposited by ALD using TEMAHf precursor and H_2O. A 300-nm Al-gate electrode was then sputtered, which was followed by lithography and dry-etching processes.

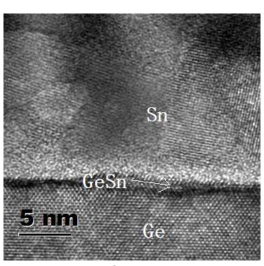

Figure 1 HRTEM image of Ge/GeSn/Sn stack

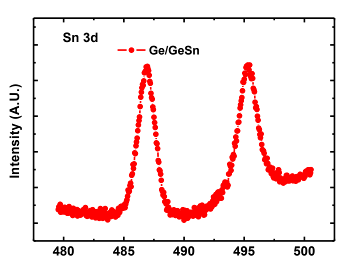

Figure 2 XPS analyse of Sn 3d spectra for Ge covered with GeSn after HCl cleaning

The cross-sectional high-resolution transmission electron microscopy (HRTEM) image of the Ge/GeSn/Sn stack, as shown in **Figure 1**, indicates that an approximately 1-nm-thick GeSn layer is generated between the Sn layer and the Ge substrate. **Figure 2** shows the Sn 3d spectrum of the GeSn surface. The Sn peak can be observed at 497.5 eV for the samples. This indicates that, there are still Sn atoms on the Ge surface after HCl cleaning. Based on XPS data, the Sn and Ge atom concentrations are estimated to be 5.7% and 40.1%, respectively.

The EOT value is about 2.4 nm for the Ge/GeSn/HfO_2/Al capacitors. And as shown in **Figure 3**, for the Ge/GeSn sample with sulfur passivation, well shaped C-V curves are obtained without significant frequency dispersion, stretch-out, or bumps near the flatband voltage. The densities of the interface states are estimated from conductance measurements to be approximately 5.3×10^{11} $cm^{-2}eV^{-1}$ for the samples.

As shown in **Figure 4,** the leakage current density of the GeSn sample with sulfur treatment is lower than 2.2×10^{-7} A/cm^2 in the voltage ranges of 1 to -1V.

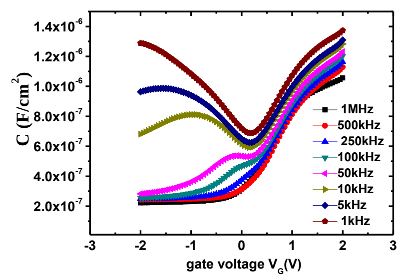

Figure 3 Capacitance-voltage (C-V) characteristics of Ge/GeSn/HfO_2/Al with sulfur passivation

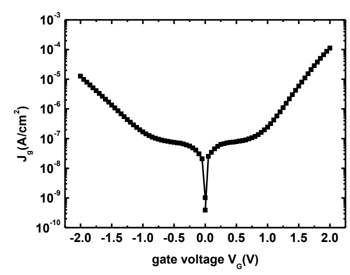

Figure 4 Leakage current density-voltage (J-V) characteristics of Ge/GeSn/HfO_2/Al with sulfur passivation

It was demonstrated that sulfur passivation for the GeSn/high-k interface leads to excellent electrical characteristics, with D_{it} reduced to 5.3×10^{11} $cm^{-2}eV^{-1}$. It was confirmed that a thin GeSn interlayer was formed at the Ge surface through the method. Electrical measurement results clearly demonstrated that sulfur treatment of the Ge/GeSn surface achieved by this method represents a promising method for improving the interface quality of the gate stacks.

Acknowledgments

This work is supported in part by the State Key Development Program for Basic Research, China (2011CBA00602), and by the National Science and Technology Major Project, China (2009ZX02035-004-01, 2011ZX02708-002).

References

[1] O. Nakatsuka, N. Tsutsui, Y.Shimura, S. Takeuchi, A. Sakai, S. Zaima, Jap. J. Appl. Phys. 49 (2010) 04DA10.
[2] G. Han, S. Su, C. Zhan, Q. Zhou, Y. Yang, L. Wang, P. Guo, W. Wei, C. P. Wong, Z. X. Shen, B. Cheng,Y. –C. Yeo, IEEE Electron Devices Meeting (2011) 16.7.1.
[3] R. Xie, C. Zhu, IEEE Electron Dev. Lett. 28 (2007) 976.