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Investigation on oxygen diffusion in a high-k metal-gate stack for advanced CMOS Technology by XPS

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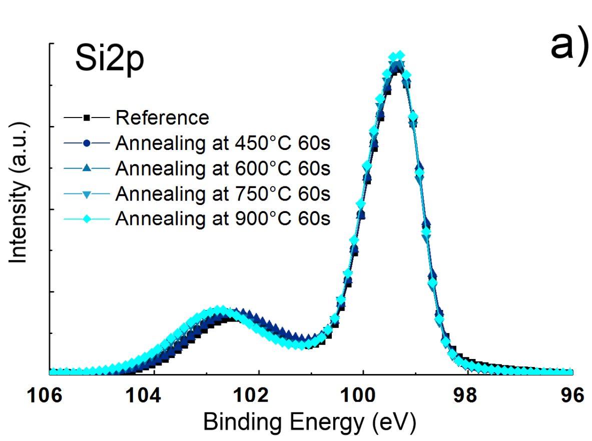
In the late 2000s' the 32nm Coupled Metal Oxide Semiconductor technology node required the use of a high-k dielectric with a metal gate instead of the historically used silicon dioxide and polysilicon. The aim was to reduce the leakage current between the gate and the channel which became critical for silicon-based gate stacks [1]. However using a high-k metal-gate architecture makes the control of the electrical properties of the transistor really challenging. Indeed the high-k material strongly interacts with its environment during the manufacturing process, which thoroughly changes the device properties.

Parameters such as the threshold voltage or the Equivalent Oxide Thickness are not only related to a material selection, but are also subject to modification due to the oxygen diffusion throughout the stack [1]. It has been shown that the oxygen diffusion leads to film thickness modifications, which have a direct impact on these properties [2]. The understanding of the oxygen diffusion dynamics hence becomes mandatory.

Our work has been performed inside a cutting-edge STMicroelectronics cleanroom. It focuses on the annealing effects with regard to the oxygen diffusion throughout the stack $TiN/HfO_2/SiO_2/Si$. For that purpose, a blank 300mm Si (100) wafer undergoes an oxidizing wet treatment (HF-SC1) to form an 8Å-thick chemical oxide layer on its surface. 2nm of HfO_2 are deposited onto this wafer by MOCVD with an Applied Material Centura (precursors TDEAH, O_2). The annealing processes are made at low pressure (5 torr), with a N_2 saturated atmosphere containing 1ppm of O_2, at 450°C, 600°C, 750°C and 900°C for 60 seconds. The experiment is renewed with 2nm of TiN deposited on the top of the stack by RF-PVD with an Applied Material Endura tool at low temperature (< 50°C), in order to avoid any thermally activated parasitic reactions. All the samples are characterized with a ReVera VeraFlex II XPS tool as fast as possible after the annealing process.

The results show that the annealing without the TiN metal has no noticeable effect with regard to oxygen diffusion, especially at the HfO_2 – substrate interface. However as soon as TiN is deposited, the Si2p spectra show an increase of the characteristic signature of SiO_2 after annealing at any temperature as shown on figure 1.



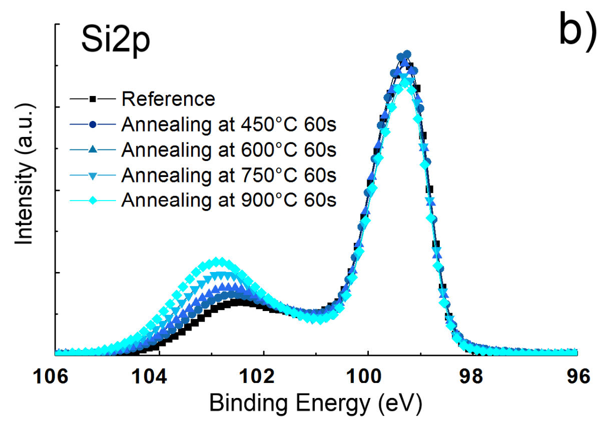


Fig. 1 XPS spectroscopy of a) HfO_2 (20Å)/SiO_2 (8Å)/Si and b) TiN/HfO_2 (20Å)/SiO_2 (8Å)/Si (20Å), stack after heat treatment in N_2 for 60 seconds at various temperatures. Focus on the Si2p region

This clearly indicates the diffusion of some oxygen towards the silicon substrate. Besides, Hf4f spectra show no major changes, but the Ti2p spectra decomposition reveals that the Ti-O component decreases with the annealing process for all the temperatures as shown on figure 2.

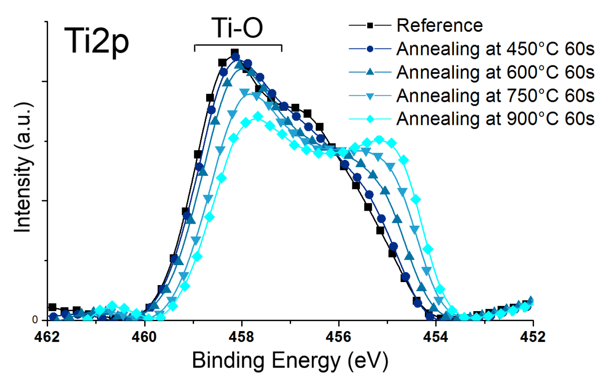


Fig.2 XPS spectroscopy of a TiN (20Å)/HfO_2 (20Å)/SiO_2 (8Å)/Si stack after heat treatment in N_2 for 60 seconds at various temperatures. Focus on the Ti2p region

Our hypothesis is that an equilibrium exists between the reduction of the native TiO_2 oxide on top of the TiN by the substrate, and the oxidation of the TiN by the ambient O_2. The TiN splits up the ambient O_2 into a monoatomic oxygen, which will migrate across the HfO_2 layer towards the substrate. This effect is discussed as a function of the HfO_2 layer thickness and the annealing duration.

We finally propose a discussion based on the existence of a battery-like electrochemical system formed by electrochemical couples separated by a solid electrolyte (HfO_2). Electrodes are formed as a gas-metal electrode formed by the TiN-N_2-: 1 ppm O_2 separated from the Si/SiO_2 redox system. This stack accelerates the oxidation of the silicon.

[1] J. Robertson, *«Fermi level pinning by defects in HfO2-metal gate stacks»*, Applied Physics Letters **91** (2007), 132912
[2] K. Kakushima et al. *«Origin of flat band voltage shift in HfO2 gate dielectric with La2O3 insertion»*, Solid-State Electronics **52** (2008) 1280–1284