Resistive switching in metal oxides: from physical modeling to device scaling

D. Ielmini, S. Balatti and S. Ambrogio
DEIB – Politecnico di Milano and IU.NET
Piazza L. da Vinci 32 – 20133 Milano – Italy

The resistive switching memory (RRAM) is one of the most promising candidate for future high-density non-volatile storage [1]. The simple 2-terminal structure, the fast switching and the low-power operation may allow a unique opportunity for NAND-replacement, as well as a potential candidate for future DRAM and logic circuits. To support material engineering and device scaling, however, the switching phenomena and their variability at the nanoscale must be carefully understood and modeled.

Resistive switching in RRAM relies on the nanoscale phenomena of ionic migration and electron conduction at a conductive filament (CF). The latter is formed by an initial breakdown to initialize the RRAM operation. Fig. 1a shows the typical I-V curve for a bipolar RRAM consisting of a HfO_2 layer interposed between two TiN electrodes. A Ti layer is interposed between the HfO_2 and the TiN top layer, to scavenge oxygen and generate defects contributing to ion migration. In the set transition at positive voltage, ionized defects migrate from the reservoir at the TE side, resulting in the growth of a CF. The resistance of the CF is controlled by the maximum current I_C during the set transition, because the voltage across the device remains fixed to a value V_C maintaining ion flow, thus resulting in a value $R = V_C/I_C$ [2]. The relationship between R and I_C is shown in Fig. 1b for a one-transistor/one-resistor (1T1R) structure, where I_C is determined by a transistor in series with the RRAM.

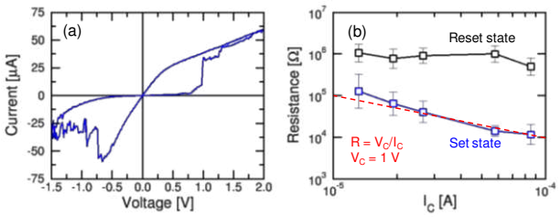

Fig. 1: I-V characteristics for a 1T1R structure (a) and measured set and reset resistance as a function of I_C (b).

The reset transition in Fig. 1a consists of an increase of the resistance due to CF disconnection. To investigate the physical mechanism of the reset process, ion transport within the CF was simulated by the drift-diffusion equation, where the ionic current j_D is given by:

$$j_D = -D\nabla n_D + \mu n_D F, \quad (1)$$

where D is the ionic diffusivity, μ is the ionic mobility, n_D is the density of ionized defects and F is the electric field [3]. The Einstein relation $D = \mu kT$ was enforced between D and μ, which were both assumed to be controlled by temperature through the Arrhenius law. Eq. (1) was solved with a finite element method with the continuity equation for electrical current and the Fourier equation for heat transport, to allow calculation of the current and of the consequent Joule heating, resulting in a local temperature increase during set and reset. Since drift and diffusion in Eq. (1) are driven by field and temperature, which are both controlled by the voltage across the device, voltage has the leading role in driving set/reset processes in the RRAM [4].

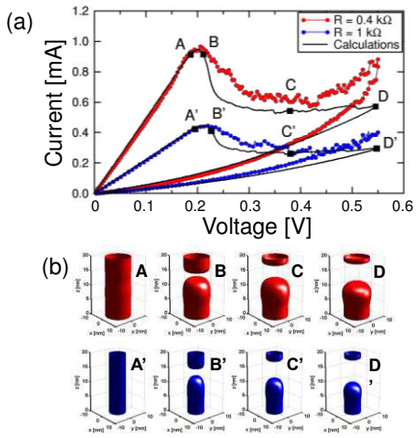

Fig. 2: Measured and calculated reset I-V curves (a) and contour plots of n_D for increasing increasing bias (states A, B, C, D) and for different I_C (red and blue plots) (b).

Fig. 2 shows the measured and calculated I-V curves for the reset transition in a bipolar RRAM. Note that the device operated with opposite polarity with respect to Fig. 1a, which accounts for the reset transition at positive voltage. The two curves were obtained after a set transition at two different values of I_C, thus resulting in different R. Fig. 2b shows the calculated contour plot of n_D for four bias points along the reset transition. As the voltage increases, ionized defects migrate toward the bottom electrode, leaving a depleted gap with increasing size. The low n_D in the depleted gap is responsible for the high resistance in the reset state.

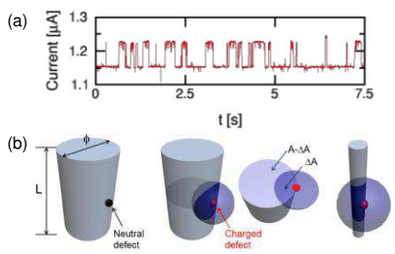

Fig. 3: Measured RTN noise (a) and sketch of the effect of charge trapping on CFs with different sizes (b).

A key requirement for RRAM is scalability, which would allow the successful replacement of an existing technology (e.g., NAND) for a sufficient number of technology nodes. Although RRAM has several key scaling advantages, such as the 2-terminal device architecture and the controllable power consumption in Fig. 1a, scaling issues exist such as random telegraph noise (RTN) [5] and switching variability [6]. RTN increases for decreasing size of the CF, as shown in Fig. 3: trapping/detrapping at the CF surface induces charge depletion and a consequent change of resistance. As the CF becomes comparable to the Debye length, full depletion takes place, which can induce a giant fluctuation of current in the device. Programming algorithm and material engineering might provide beneficial effects to variability and noise, thus boosting the scaling capability of RRAM.

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