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Monolithic Integration of High Temperature Silicon Carbide Integrated Circuits

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Silicon Carbide (SiC) has received a special attention in the last decades thanks to its superior electrical, mechanical and chemical proprieties. Nowadays, SiC is mostly used for applications where Si is limited, becoming a proper material for both unipolar and bipolar power device applications under high power, high frequency and high temperature conditions. Aside from the outstanding theoretical and practical advantages still to be proved in SiC devices, the need for more accurate models for the design and optimization of these devices, along with the development of integrated circuits (ICs) on SiC is indispensable for the further success of modern power electronics. The design and development of SiC ICs has become a necessity since the high temperature operation of ICs is expected to enable important improvements in aerospace, automotive, energy production and other industrial systems. Due to the last impressive progresses in the manufacturing of high quality SiC substrates, the possibility of developing new circuit applications is now feasible. SiC unipolar transistors, such as JFETs and MESFETs show a promising potential for digital ICs operating at high temperature and in harsh environments.

This paper presents a complete fabrication cycle starting with the SiC MESFET design, process technology setup, circuit's design using SPICE, and finally the fabrication and testing of the elementary logic gates library. This library allows implementing multi-stage logic embedded in power management circuitry. Our preference for MESFETs is due to the already proved stability of the Tungsten-Schottky barrier. We have successfully employed this technology in the fabrication of stable SiC Schottky diodes for the space mission BepiColombo [1].

The reported ICs on SiC have been realized so far with either a small number of elements, or with a low integration density [2, 3]. Therefore, the first step was to develop a new 4H-SiC MESFET specially suited for large ICs development. As the final purpose of the new MESFET is to be embedded in further circuit designs, it appeared the necessity to accomplish the main circuit's requirements, generally applicable to Si ICs: wafer planarity and device scalability. The N-wells isolation technique [4] and the finger-gate device design has been adopted, techniques widely used in Si CMOS ICs. Therefore, we have successfully achieved a good surface planarization, assuring proper interconnections between different multi inter-level metals. We have also successfully realized scalable transistors and 4H-SiC epitaxial resistors. The embraced geometry presents a built-in drain-source residual current. Therefore, an additional oxide gated MESFET ×0.04 than the main MESFET was implemented under the prolonged gate metallization, in order to block any residual drain-to-source leakage current. This oxide gated MESFET was taken into consideration in the SPICE modeling.

The starting material is a 5μm thick P-layer grown on a 4H-SiC semi-insulating substrate with a doping of $N_A=5\times10^{15}$ cm^{-3}. On top of the P-layer, an N-epilayer was grown (0.5μm thick and $N_D=10^{17}$ cm^{-3}). The first step in the digital ICs design was the fabrication of the basic 4H-SiC MESFETs to extract the SPICE experimental parameters. The device model was extracted for the 25°C-300°C temperature range. The MESFET fabrication was carried out with 2μm lithography, with a total of 10 masks and three metal levels. To increase the integration density we have used two metal interconnections between devices and circuits, for which four masks (2 metals and 2 vias) were necessary. The experimental MESFET pinch-off voltage (V_P) does not depend on temperature, independently of the number of gate fingers, its value being close to -8.5V. Since these 4H-SiC digital ICs are supposed to work at high temperatures a special attention has been paid to the temperature matching between individual devices. The SiC ICs monolithically integrate MESFETs with resistors on the same chip. Therefore, for temperature matching in the circuit, the same N-type epitaxial layer for both devices has been used.

For the design and modeling of the basic logic gates we have adopted the ICs topology developed by NASA on 6H-SiC [5]. Because the MESFETs need negative voltage control and due to the lack of complementary devices, a load resistor and a level shifter are necessary in the logic gate scheme. The level shifter is made with a voltage follower and a two-resistor divider. It was designed assigning 0V for the High logic level and a value close to the MESFET V_P for the Low logic level. First, we have demonstrated the proper operation of the basic logic gates at room temperature. Furthermore, these have provided the expected functionality of complex multi-stage digital ICs using standard CMOS topologies [6], such as Data Flip-Flop (it contains a total of eleven 4H-SiC MESFET elementary gates). The functionality of other circuits by realizing external connections between SiC ICs has been also proved. Then, we have shown that the basic logic gates properly perform their natural function up to 300ºC. Although at temperatures above 200ºC the output level response of the gates starts drifting negatively, the logic gates operate in the acceptable operation range. This behavior is mainly explained by the level shifter evolution in temperature. As the voltage follower transistor works always in saturation, at higher temperatures the drain-gate leakage current significantly increases. Therefore, the follower experiments an additional voltage drop, hence drifting negatively the MESFET gates logic output levels. However, by using a higher Schottky barrier for the MESFET gate contact, the output negative drift of the 4H-SiC logic gates can be easily minimized for higher temperature operation.

Multi-stage digital circuits, elementary logic gates, a voltage reference analog circuit and a power MESFET have been monolithically integrated on the same wafer. In summary, we can confirm that our MESFET ICs technology enables the fabrication of mixed signal ICs that are capable to operate at high temperature.

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