Abstract #2190, 224th ECS Meeting, © 2013 The Electrochemical Society

Electrical Properties and Charge Transport in the Pd/Al_2O_3/InGaAs MOS Structure

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High mobility channel material such as high In-content InGaAs is considered as a potential candidate for replacing strained Si in future CMOS devices [1]. The use of high-κ dielectric materials in conjunction with the III-V channel region is required to realise MOSFET structures. We present results of electrical characterization and the determination of the dominant transport mechanism in the Pd/Al_2O_3/$In_{0.53}Ga_{0.47}As$/InP MOS system. The high-κ Al_2O_3 oxide layer of the MOS capacitor structure was formed by an ALD process with nominal physical thickness t_{ox} of 5, 10, 15 and 20 nm. Prior to gate oxide deposition the $In_{0.53}Ga_{0.47}As$ surface was passivated by an immersion in 10% $(NH_4)_2S$ solution at room temperature for 20 min. The samples received no post-metallization annealing treatment. Samples with both *n(S)*- and *p(Zn)*-type doped ($4x10^{17}cm^{-3}$) $In_{0.53}Ga_{0.47}As$ epitaxial layers were characterized by capacitance-voltage (*C-V*), current-voltage (*I-V*) measurements over the temperature range of 100 – 300 K.

Fig. 1 presents current density (*J*) vs. gate bias plots for *p*-MOS structures with different Al_2O_3 thicknesses. The similarity of the *J-V* curves for both types of the substrates (not shown here) and the general shape of the characteristics are consistent with a current transport mechanism governed by electron tunneling through the triangular potential barrier at the metal-dielectric or semiconductor-dielectric interface. In this case, the current can be described by Fowler-Nordheim (FN) tunneling [2]. The potential barrier φ_B responsible for the carrier transport can be found from the slope of FN plot ($\ln(J/E^2)$ vs. $1/E$) [3].

FN plots of the *p*-type MOS capacitor are shown in Figs. 2-3. The samples with t_{ox}= 5 nm do not show a well formed barrier at the interfaces possibly due to the dominating of direct tunneling transport mechanism. For the case of electron tunneling from the metal electrode (Fig. 2), the barrier height is the same for the 10, 15 and 20 nm thick dielectric and φ_B equals to 2.40±0.10 eV. For the electron tunneling from the semiconductor (Fig. 3), 10 nm thick dielectric gives the conduction-band energy offset at the Al_2O_3/InGaAs interface φ_B=2.50±0.06 eV, which is in a good agreement with the results reported in [4, 5]. From Fig. 3 it is evident that the barrier heights (φ_B) exhibit an apparent reduction with increasing film thickness. This could be explained by formation of a transition layer in the Al_2O_3 film due to increased time of dielectric deposition. Also previous analysis has demonstrated that Al_2O_3 deposited by ALD on $In_{0.53}Ga_{0.47}As$ surfaces exhibits a fixed positive charge distributed throughout the oxide [6]. This positive charge would modify the barrier at the injecting interface resulting in an apparent reduction in the barrier height with increasing oxide thickness. *C-V* response (see Fig. 4) was recorded after each *J-V* sweep at the same temperature conditions. It was found that no degradation and non-reversible charge trapping in the dielectric occurred.

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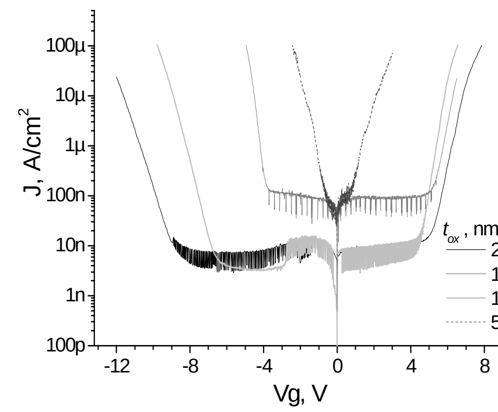

Fig. 1. *J-V* plot for MOS capacitors with *p*-type substrate.

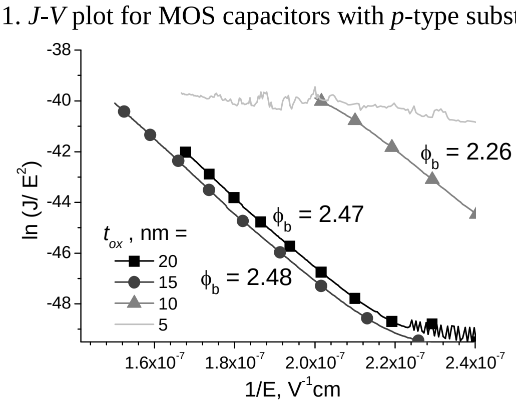

Fig. 2. The FN plot of *J-V* characteristic (V_g <0) of Pd/Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$/InP structure.

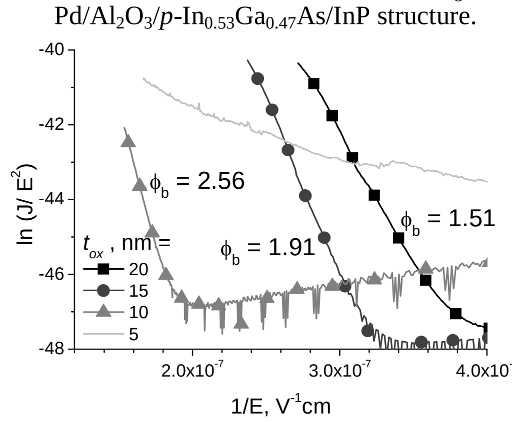

Fig. 3. The FN plot of *J-V* characteristic (V_g>0) of Pd/Al_2O_3/*p*- $In_{0.53}Ga_{0.47}As$/InP structure.

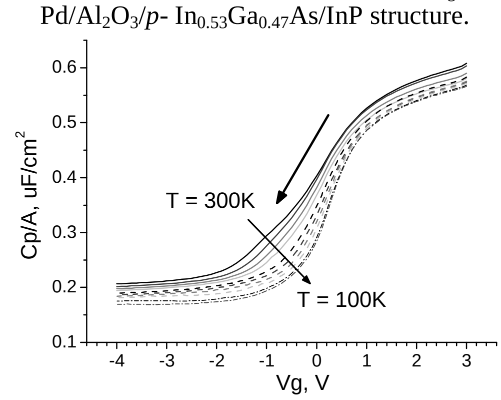

Fig. 4. 300kHz *C-V* response of *n*-MOS capacitor with t_{ox}=10 nm measured at temperature range of 100 – 300 K.