Improved Operation Characteristics in Charge-Trapping Flash Memory Devices with Engineered Dielectric Stack, SiGe and Junctionless Poly-Si Channels

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Charge-trapping flash (CTF) memory devices with high-k trapping layer have been frequently discussed [1-9]. The programming characteristics of these devices can be enhanced by the high-k charge-trapping layer due to its larger trap density and smaller band offset to Si. However, the retention characteristic is still an issue [7-9] because high-k material suffers lower crystalline temperature and shallower defect level. Therefore, a Si_3N_4/high-k material stacked charge-trapping layer was proposed to improve the retention characteristics, since Si_3N_4 has deeper trap level, higher crystalline temperature and it provides an effective barrier for high-k material such as HfO_2 [10]. Moreover, faster erase speed also can be achieved by its smaller valence band offset for Si_3N_4 to Si. In addition, it was reported that the multi-level cell characteristics can be obtained by inserting Al_2O_3 into Si_3N_4 (i.e. Si_3N_4/ Al_2O_3/Si_3N_4 trapping layer) due to the modulated trapping charge distribution [11]. However, since Si_3N_4 is the major trapping-layer material, the scaling down for device is limited [12]. Instead, CTF devices with Si_3N_4/Al_2O_3/high-k charge-trapping layer is proposed and investigated in this work. Double layers with various high-k films on Si_3N_4 are compared first. Then, triple layers with Si_3N_4/various high-k/HfO_2 are investigated.

Some approaches such as stacked high-κ blocking/charge-trapping layers [8,13], stacked tunneling layers [14,15], and the utilization of SiGe buried channel [16-20] have been reported to enhance operation characteristics in CTF devices. Among them, the utilization of SiGe buried channel is considered the most promising for improving the performance and lowering the operation voltage, according to simulations [17,18]. Employing a strained pseudomorphic SiGe layer as a high-mobility channel for MOSFETs has been widely reported. Its easy-fabricating and compatibility are helpful in CTF memory applications. However, relevant experimental results are rarely reported. P-channel CTF devices can be operated by hot-electron injection with junction avalanche to achieve efficient programming [21]. In this work, the operation characteristics as well as the reliability properties of p-channel CTF transistor devices with different Ge contents in SiGe buried channel are experimentally investigated. P/E speeds, retention and endurance of devices with SiGe buried channel are compared to the one with conventional Si-channel.

A stacked Si_3N_4/HfO_2 charge-trapping layer was proposed to improve erase operation and retention for CTF device. The improvement can be attributed to the smaller valence band offset of Si_3N_4 to Si and the higher barrier for electrons detrapping from HfO_2 to Si_3N_4. Programming and retention characteristics of CTF devices can be further enhanced by inserting Al_2O_3 between Si_3N_4 and HfO_2 as the charge-trapping layer. This is because most of the injecting charges are trapped at Si_3N_4/ Al_2O_3 interface and Al_2O_3 also provides a high barrier for electron detrapping.

Operation characteristics of p-channel TaN/ Al_2O_3/HfO_2/$HfAlO_2$/SiO_2/Si MAHOS-type CTF memory devices with different Ge contents in SiGe buried channel are investigated in this work. Compare to those with conventional Si-channel, both programming and erasing speeds are significantly improved by employing a $Si_{0.7}Ge_{0.3}$ buried channel. Satisfactory retention and excellent endurance characteristics up to 10^6 P/E cycles with 4.1 V memory window show that the degradation on reliability properties, if it exists, is negligible when SiGe buried channel is introduced.

A junctionless (JL) polycrystalline silicon (poly-Si) flash memory device with HfO_2/Si_3N_4 (HN) stacked trapping layer is studied for the first time. Effects of the HN stacked trapping layer on JL and inversion-mode (IM) flash devices are compared. JL device shows faster programming speed than the IM one because of its heavily doped n-channel. Specially, comparable erasing speed of JL device can be achieved by HN stacked trapping layer due to more effective electron de-trapping. JL device with HN stacked trapping layer also shows better retention characteristics and keeps a larger window after 10^5 programming/erasing cycles, which makes it promising for three-dimensional (3-D) memory integration in the future.

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