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Optimization of W\Al_2O_3\Cu(-Te) material stack for high-performance conductive-bridging memory cells

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Over these last years the memory market has been steadily expanding, mainly due to the boom of portable applications such as smart phones. Flash technology still dominates this market, however will face physical limitations with further cell scaling. On the other hand, better scalability is expected for resistive RAM (RRAM) concepts based on nano-sized filamentary switching. Between the different technologies, the conductive-bridging memory (CBRAM), also termed electrochemical metallization memory (ECM), is a very attractive concept offering low write power and long endurance [1-2].
CBRAM operation relies on the voltage-induced electrochemical formation and rupture of a Cu- or Ag-based conductive filament through an insulating layer used as solid state electrolyte for cation drift. The resulting reversible bridging between the two electrodes allows controlled resistive switching between a high-(HRS) and a low-resistive state (LRS). While elemental Cu or Ag is typically used as cation-supply elements, chalcogenides such as GeSe or GeS are most often considered as electrolytes due to the high mobility of Cu or Ag in these materials, allowing thus fast programming.

Our approach is to *explore alternative materials both for the cation-supply and the electrolyte elements*, with the two-fold purpose of *facilitating the cell integration* and of *optimizing the memory characteristics and reliability*.
We obtained promising CBRAM properties using CMOS-friendly *thin amorphous A_2lO_3 layers* prepared by the atomic-layer-deposition method, and sandwiched between a W bottom electrode and either *a pure-Cu or a Cu-Te* compound cation-supply layer.
The W\Al_2O_3\Cu(-Te) CBRAM cell is integrated in a 1-Transistor/1-Resistor (1T1R) configuration, whereby the 90nm W-plug serving as bottom electrode is stacked on the drain [Fig. 1(a)].

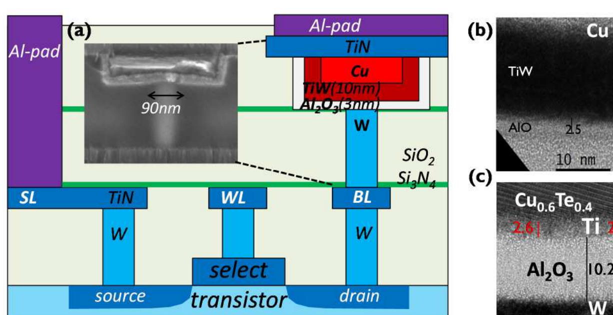

Fig. 1. (a) schematic structure of a 1T1R CBRAM cell; inset shows a Al_2O_3\TiW\Cu cell stacked on 90nm W-plug; (b) close-up of the stack; (c) alternative structure consisting of a Al_2O_3\Ti\Cu-Te stack

After deposition and patterning of a TiN top electrode, Si_3N_4- and SiO_2-based passivation layers are deposited at ~400°C followed by Al bond-pad processing. In order to limit the in-diffusion of Cu induced by this integration thermal budget, it is required to develop *appropriate Cu-buffer* layers. We investigated the buffering properties of *thin Ti, Ta or TiW* metallic liners, by means of different complementary approaches. In this respect, the internal photoelectron spectroscopy (IPE) technique proved very useful, because the measured metal/oxide electron barrier height is drastically affected if Cu material, having large work-function (WF), has diffused through a low-WF liner material like Ti. By this method we could evidence *lower Cu in-diffusion from a Cu-Te source compared to a pure-Cu source* [Fig. 2(a)]. Corroborating IPE results, ToF-SIMS characterization also made it possible to *adjust the thickness of the liner* so as to keep the level of in-diffused Cu reasonably low after anneal [Fig. 2(b)].

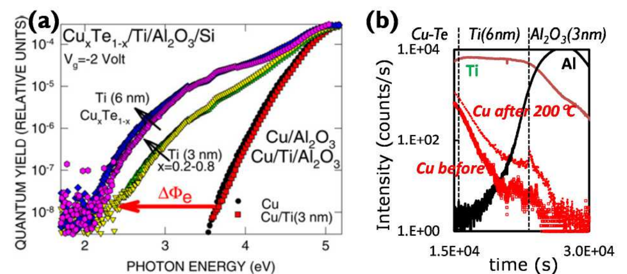

Fig. 2. (a) example of IPE responses obtained for different stack configuration, showing a decrease of the electron barrier for thicker Ti liner inserted at the Al_2O_3\Cu-Te stack; (b) ToF-SIMS depth profiles obtained for as-prepared and annealed Si\Al_2O_3\Ti\Cu-Te stack, showing limited Cu in-diffusion

Not only Cu in-diffusion should be looked after through integration thermal budget, but also the homogeneity of the composition and microstructure of Cu-Te alloys. We optimized these latter aspects through *composition tuning, process developments, as well as doping investigations*. As a result, integrity of Al_2O_3\Cu-Te based cells is preserved after annealing up to ~400°C.

High control of electrical-switching properties is obtained both on Al_2O_3\Cu and Al_2O_3\Cu-Te based cells, using different types of liner materials. Fig. 3(a) shows typical quasi-static switching loops obtained for a 90nm-size integrated W\Al_2O_3\Cu cell. Excellent pulse-programming characteristics are also assessed, showing 10ns-fast and <3V write pulses, multilevel functionality, and low-current operation (10µA). Cells also exhibit remarkable voltage-disturb immunity, as well as excellent endurance characteristics over 10^6 set/reset cycles [see Fig. 3(b)].

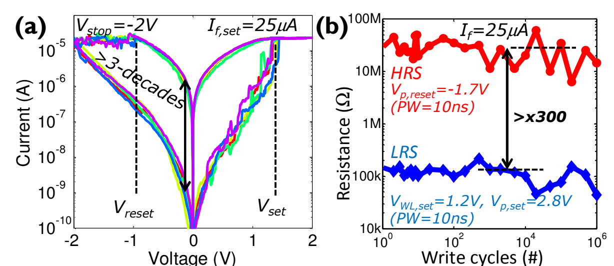

Fig. 3. (a) typical switching characteristics obtained using a current $I_{f,set}$=25µA controlled by transistor during forming/set, and showing a 3-decade memory window; (b) write endurance characteristics performed using 10ns-long pulses without verification loop, and showing stability >2 decades window up to >10^6 set/reset cycles

In this paper we will present the *optimization steps* addressed for the different types of material stacks, and we will discuss the *electrical properties* based on structure variations as well as *correlations with physical analyzes and modeling studies*

References

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