Leakage Current Analysis Depends on Grain Size Variation in Zinc Oxide Thin Film Transistor

Hojoong Kim, Suk Yang, Kyung Park, Parthiban Shanmugam, and Jang-Yeon Kwon
School of Integrated Technology, Yonsei University, Incheon, 406-840, Korea

Oxide semiconductor based thin film transistors (TFTs) provide an alternative to replace amorphous silicon based devices due to a higher mobility (5 ~ 30 cm^2/Vs), possibility to low temperature process, and potential to apply for transparent devices [1]. Amorphous indium gallium zinc oxide (a-IGZO) is the representative of the oxide material that has a good mobility (~10 cm^2/Vs) in the amorphous phase, stable and uniform film characteristics [2]. However, it contains several challenges, especially limitation of improving mobility that brings about the difficulty to utilize for the high performance TFTs. Zinc oxide (ZnO) which is a base material of oxide semiconductor has high hall mobility comes from the 4s orbital overlapping characteristics, rendering expectation of high motility. However, it is difficult to generate an amorphous ZnO film because it easily forms polycrystalline structure at the room temperature. In this work, ZnO grains are reduced using various processes toward the amorphous structure and analyzed how these affect to the TFT's electrical characteristics.

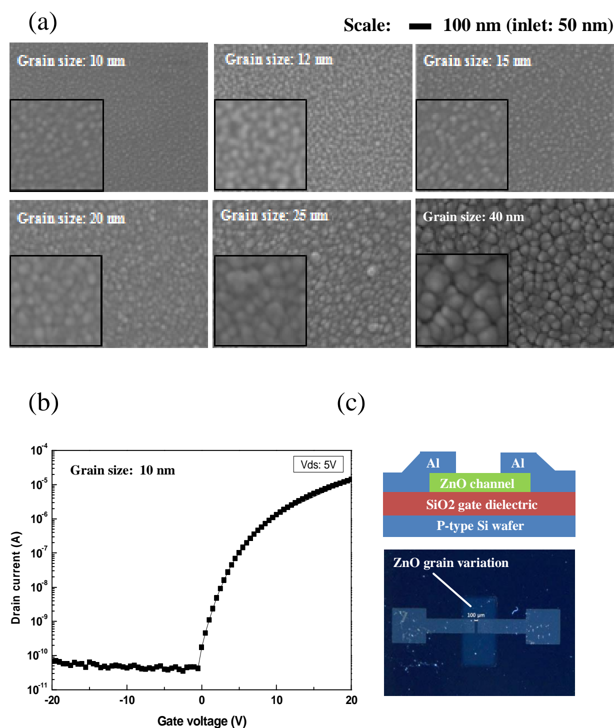

Figure.1. (a) SEM images of the ZnO TFT's channel layer with different grain sizes (10, 12, 15, 20, 25, and 40nm), (b) Transfer curve of 10nm grain ZnO TFT and (c) it's schematic diagram

ZnO TFTs are fabricated as a bottom-gate structure that constituted dry oxidized SiO2 gate insulator (100nm) on the highly doped p-type silicon wafer as a gate electrode. ZnO layer is deposited by rf sputtering with changing variables related to define the grain size, which are sputter power (50 to 600W), film thickness(50 to 240nm), working pressure (5 to 20mTorr),and oxygen partial pressure (0.5 to 10%), respectively. After Al source and drain electrodes (100nm) deposited by dc sputter, all TFTs are annealed at 200°C in the atmosphere environment for 1 hour.

ZnO TFTs are fabricated with various grain sizes of ZnO film, which have from 10 to 40 nm of scale. Figure 1(a) shows SEM images to find out the ZnO grain structure and figure 1(b) is a 10 nm grain size ZnO TFT's transfer curve. It is hard to find a correlation with grain size variation and mobility, but the off-currents are decreased from 3.55 x 10^{-11} to 4.90 x 10^{-13} A, two orders of magnitude with increased grain's dimensions as shown in figure 2(a).

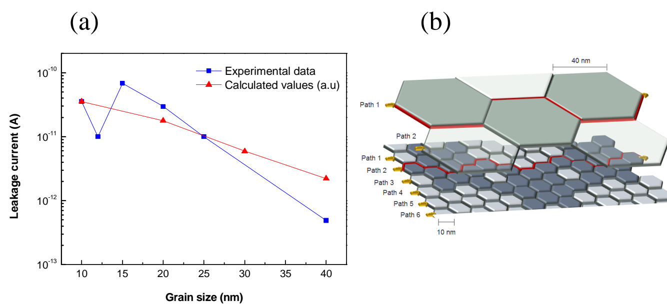

Figure.2. (a) Leakage currents of the ZnO TFT from the experiment and modeled data and (b) ZnO grains (10, and 40 nm of size)

The leakage current is calculated as a function of the grain size, based on several assumptions. At first, grains are shaped as a regular hexagonal structure (Figure 2.b). Second, the leakage current flows along the path of grain boundaries on the shortest way and which through the bulk is not concerned. Lastly, the leakage current is calculated by a proportion to the number of grain path divided the distance of the shortest path. As the grain size is increased, the number of path is decreased exponentially, but the distance of grain path is same result with the grain size, interestingly. Figure 2(a) shows the leakage current of the experimental data and calculated values with grain size increases. As the grain size is increased from 10 to 40 nm, the calculated leakage current is decreased from 3.55 x 10^{-11} to 2.22 x 10^{-12} A. The results of the graph indicate that increasing number of grain due to the shrink of grain size influences the TFT's off-current characteristics.

In summary, ZnO TFTs are fabricated in the various process conditions of sputtering in order to decrease grain size for uniformity and find out how it affects to the devices' electrical characteristics. Amorphous ZnO would be guaranteed the high mobility and good uniformity, however it is concerned about the leakage current increase thus continuous and intensive study should be needed.

[1] J. –Y. Kwon *et al*. Electrical Materials Letters, Vol.7, No. 1(2011), pp. 1-11
[2] T. Kamiya *et al*. Sci. Technol. Adv. Mater. 11 (2010) 044305