Triangular Voltage Sweep Measurements after Current-Ramp Temperature Stress

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New barrier processes are currently being screened in order to identify the most promising candidates for reducing the barrier thickness in Cu damascene interconnects [1]. As an example, Mn-based self-forming barriers are being considered as a possible option to enable barrier thickness scaling to 1 nm and below [2]. When the barrier thickness reduces, barrier integrity and uniformity across the wafer become critical for meeting the reliability requirements.

Time Dependent Dielectric Breakdown (TDDB) measurements are typically used for dielectric reliability assessments [3]. However, TDDB tests can only assess the overall reliability of the investigated interconnect schemes, while the main cause of the detected failures remains questionable. In particular, early failures can originate either from a defective barrier or from a degraded dielectric. If the barrier is discontinuous or presents pinholes, Cu can drift into the interconnect dielectric and lead to shorts between Cu wires. If the dielectric gets damaged during the integration process, the related strength reduces and early breakdowns occur. The latter is especially true for highly porous low-k materials with ultra-low relative dielectric constant (k-value), which are more prone to degrade during processing. In the optimization phase of an advanced barrier process it is fundamental to understand whether poor TDDB performance are due to defects in the Cu barrier or to process-induced damage in the interconnect dielectric.

In this work, Triangular Voltage Sweep (TVS) measurements after Current-Ramp Temperature Stress (CRTS) were evaluated as a methodology to discriminate between barrier-related and dielectric-related degradations. Fig. 1a shows the schematic cross-section of the Metal-Insulator-Metal (MIM) structures we used to assess the methodology. These are trench capacitors, which are particularly suited for screening new barrier processes, as they allow evaluating the intrinsic reliability of barrier/dielectric stacks [4]. The measurement configurations are reported in Fig. 1b and Fig. 1c. In the CRTS phase, a current ramp is forced at high temperature (e.g. 200ºC) in order to promote Cu drift into the dielectric and, thus, challenge the capability of the investigated barrier to contain Cu (Fig. 1b). As the forced current increases linearly with time, leakage-induced voltage saturation can be avoided (or significantly delayed), which makes CRTS more effective than constant-current temperature stress [5]. In the TVS phase, a double voltage sweep with changing polarity is applied to detect possible injected Cu (Fig. 1c). When Cu drift occurs, the measured voltage in CRTS drops to a lower level (Fig. 2b), while the measured current in TVS shows a peak, typically preceded by an initial bending of the trace (Fig. 2c) [6]. After that the initial state is restored, as the second TVS matches the initial one before CRTS. These features in the CRTS and TVS traces are peculiar to Cu drift, as it was verified by comparing samples where Cu drift was expected (e.g. the barrier was discontinuous or intentionally omitted) with samples with an outstanding barrier or without Cu (i.e. Cu drift could be excluded). In fact, when Cu drift is not involved, the measured voltage in CRTS drops to 0 Volt (Fig. 3b) and the measured current in TVS reaches meter compliance, which indicates dielectric breakdown (Fig. 3c). Such behavior is distinctive and can be used to associate possible early failures to a degraded dielectric with a reduced dielectric strength. CRTS-TVS measurements were used to assist the optimization of various barrier processes. Fig. 2 and Fig. 3 show the case of Mn-based barriers on low-k (k=2.5) and oxide films, respectively. These samples are only a showcase for the methodology and the reported results should not be considered representative for the final barrier process. Based on the CRTS-TVS results, it was possible to conclude that for the low-k sample the poor TDDB performance in Fig. 2a originated from a defective barrier, which needed further optimization. For the oxide sample, CRTS-TVS further validated the good quality of the barrier (Fig. 3).

We conclude that CRTS-TVS measurements represent an effective methodology for investigating failures in 2D and 3D interconnects and in particular identifying defective Cu barriers.

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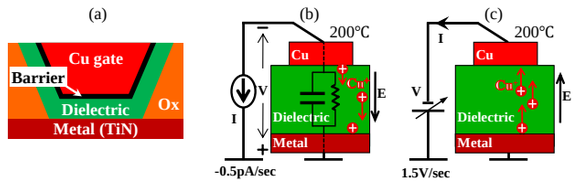

Figure 1 Trench capacitors (a) and circuit schematics for CRTS (b) and TVS measurements (c)

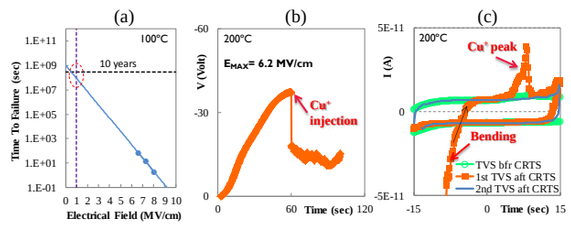

Figure 2 TDDB tests (a), CRTS (b) and TVS measurements (c) on Cu/6nm Mn barrier/60nm Low-k 2.5 trench capacitors

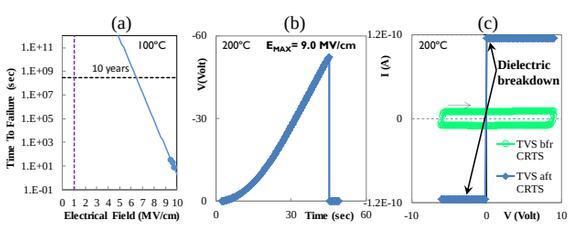

Figure 3 TDDB tests (a), CRTS (b) and TVS measurements (c) on Cu/1.2nm MnN barrier/60nm Oxide