Electroless Deposition on self-assembled monolayers as a method to enable fabrication of advanced interconnects

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Density scaling of integrated circuits for future electronic devices presents some manufacturing challenges.

For Example, the classic thin film deposition techniques used in the fabrication of the back-end-of-line interconnects, such as PVD (Physical vapor deposition), are not extendable for wires sizes below 20nm [1].

Robust sidewall coverage from a line of sight PVD process is difficult to achieve at small dimensions as there is a risk of feature pinch off blocking the subsequent plating and filling of the wires. This will lead to voiding and poor line resistance and reliability. On the other hand, depending on EP to fill features with thin seed could lead to sidewall voiding due to seed dissolution in the bath and large terminal effects across the wafer. The problems faced by a PVD/EP process for gap fill will be further magnified if the wafer size is increased from 300mm to 450mm. Furthermore, below the 20nm feature size, the performance of the barrier/seed/electro-plating approach is no longer acceptable. The volume taken by the barrier dramatically reduces the conductor volume .Therefore the resistivity increases exponentially with scaling.
For that reason, new approaches need to be used in order to facilitate the aggressive dimensions of new technology nodes.

Possible ways to tackle these limitations are the use of platable SAMs (self-assembled monolayers) as a path for new conformal metallization techniques such as ALD (Atomic Layer Deposition), CVD (Chemical Vapor Deposition) or EL (Electroless deposition) in order to extend copper diffusion barriers and to search for alternative metals to copper based on material properties like diffusivity into ILDs and metal resistivity [2, 3].

In this work we present Ni electroless deposition on SAMs as alternative barrier candidate against copper diffusion and an alternative to PVD/EP-fill approach for small dimensions interconnects. A catalyzed SAM layer acts as a seed for Ni electroless plating. The layer conformably grows from the sidewalls until a specific barrier thickness is achieved as shown in Figure 1 and Cu EL grows directly on the metallic barrier filling the feature with no seam. As a result of the EL implementation sub-20nm lines are filled with either Cu or Ni EL with no voiding present as shown in Figure 2 a), b) and c).

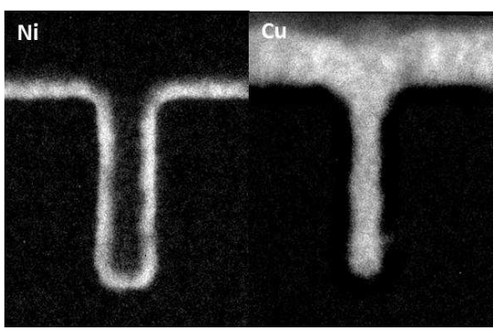

Fig. 1 EFTEM images of Ni EL barrier and subsequent Cu EL fill

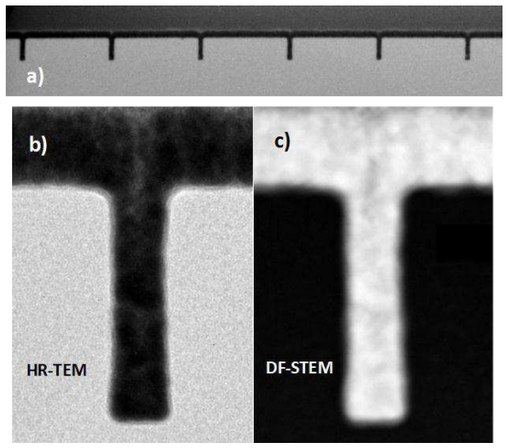

Fig. 2 Sub-20nm metal lines filled by Ni electroless on a catalyzed SAM. High resolution TEM images, a) dense lines area X-section b) isolated line X-section c) Dark Field TEM image of the isolated line X-section

The challenges of using this approach are many; among them we can stress the following ones:

1. Nucleation density on the SAM functional groups should be high enough in order to generate very thin continuous films allowing a conformal growth within a trench or a via.
2. Adhesion with the ILD and/or the SAM layer must be high enough in order to meet planarization requirements.
3. Resistivity must be competitive enough in order to act as a barrier or replace copper as an interconnect metal.

In the current study nucleation improvements of EL Ni films showed the importance of type of SAM used compared to other factors like activation or reaction times. On the other hand, the resistivity of the EL Ni films was optimized by lowering the Ni film alloying concentration. Further optimization would include both achieving higher nucleation densities in order to get a thinner continuous films and minimizing the contaminants of the Ni barrier candidate films in order to reduce resistivity.

Tape tests show good initial adhesion of both Cu-Ni- SAM-SiO_2 and the Ni-SAM-SiO_2 interfaces. This is confirmed for the Ni-SAM-SiO_2 by a successful coupon level CMP study in which silica slurry was used. CMP also requires further development and optimization.

Overall, the possibility of integrating electroless Ni barrier on SAM for the fabrication of sub-20nm Cu wires and the EL filling abilities has been demonstrated. In addition, future areas of improvement have been highlighted.

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