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Power Electronic Module Packaging at UA

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The educational and research efforts in power electronic module packaging at the High Density Electronics Center (HiDEC), University of Arkansas (UA), are described in this paper. Two courses in microelectronic packaging have been offered since 1994. As a result of these efforts, a multi-author edited textbook entitled “Advanced Electronic Packaging” was published in 1997 [1] and its second edition was published in 2006 [2]. The first course is an undergraduate/graduate introductory course covering topics such as packaging materials, processing, electrical, thermal, mechanical, and design aspects of electronic packaging, integrated passives, assembly technology, multichip/3D packaging, RF, power, and low-temperature co-fired ceramics packaging, reliability/analytical, and cost/evaluations. Some of these topics have a laboratory component to reinforce the students’ learning experience. For example, the laboratory component for the power packaging lectures involves a laboratory demonstration of the power semiconductor die attachment using a solder alloy in a chain furnace. Students are exposed to the die attachment process, including the solder reflow profile and practical operation of the reflow furnace. This course has been frequently taken by electrical engineering, mechanical engineering, and microelectronic-photonics students over the years. The pre-requisite for this first course in microelectronic packaging is senior or graduate standing in engineering and science. Over the last 20 years, many highly motivated undergraduate engineering students have successfully completed this first course.

The second course is graduate level and offers opportunities for individual students to specialize in a particular packaging technology such as power electronic module packaging, high-frequency packaging, or flexible electronic packaging. In the power electronic module packaging, substrate and material selections, the attachment strategy, design/processing/assembly issues for the development of high temperature and high power silicon, silicon carbide (SiC), and gallium nitride (GaN) power electronic modules are discussed. These wide bandgap power semiconductor devices have been shown capable of operating at temperatures of 350-400°C. The requirements of operating temperatures higher than 150 ^{o}C for power electronic modules require substantial changes to conventional power module fabrication techniques and material selections. These operating environments typically desire an operating junction temperature greater than 200 ^{o}C, coupled with the need to increase power density at both the device and system level consistently extending the limits of the available power semiconductor devices, module packaging, passive and driver technology, and thermal management systems to ensure a balance of electrical, thermal, and mechanical properties over the proposed temperature range to minimize electrical power losses, minimize thermal impedance of the package and module, and provide mechanical reliability.

The need for high power, high temperature device packages and modules has led to significant research and development efforts in power electronic module packaging. At these high operating temperatures, some failure modes manifest themselves more readily. For example, passivation and encapsulations utilized for voltage isolation at both the device and module levels break down more readily at high temperatures presenting a major reliability problem for power electronic modules. The requirements for high voltage breakdown in power electronic module applications require series connection of several power semiconductor devices to increase their high voltage handling capability. The most common high-voltage press-pack power semiconductor packages are adapted from the traditional “hockey puck” packages [3]. This rigid pressure contact packaging technology, intended for the rugged silicon thyristors, is not optimized for the sensitive microstructures on the surface of modern power semiconductor devices such as wide bandgap SiC devices [3]. As a consequence, a great deal of care is required during the module assembly process. The issue is further aggravated when the press-pack module size is increased to increase current handling capabilities. There is a significant impact on system production cost as a result of these shortcomings [3]. Recent advances in high-voltage SiC and GaN power semiconductor devices require a different power module packaging approach. Currently, SiC devices are achieving breakdown voltages above 10 kV and are at the limits of traditional high-voltage packaging solutions. Cree and Powerex have developed high voltage power modules utilizing 10 kV SiC MOSFETs in a wire bonded module [4]. However, as these device breakdown voltages increase, new approaches in module package design, passivation, and encapsulation become necessary.

The UA approach examines several wire-bonded and wire-bondless module packaging architectures including the use of 8 kV rated devices with a direct solder attachment hierarchy for interconnection. This involves the use of two direct-bond copper (DBC) substrates, one acting as the power substrate connected to a copper base plate and the second as an interconnection lead-frame between the power semiconductor devices. This module configuration was chosen to maximize power density of the module while also achieving the potential for double-sided cooling. Naturally, voltage breakdown between the topside and backside of the devices is inevitable due to the small distances between them. In order to eliminate this voltage breakdown potential, UA researchers have developed a two-step passivation technique using a nano silica embedded polyamide imide layer.

References

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