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A CMOS Compatible, Forming Free TaO_x ReRAM

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Redox random access memories (ReRAM), also referred to as memristors, are a leading emerging nonvolatile memory device due to excellent scalability, compatibility with multi-layer fabrication, high endurance, and low voltage operation. Furthermore, the analog properties of this device are a potential enabler of neuromorphic computing. Of particular interest are the class of ReRAM based on the mechanism named valence change memory (VCM) and fabricated from transition metal oxides (TMOs) such as TaO_x, HfO_x, and TiO_2 [1]. Resistance switching of VCM ReRAM is the subject of continued research, but is thought to occur as a result of oxygen vacancy motion in a small (50-200 nm) channel created in the TMO region of the device [1]. This particular class of ReRAM has achieved record endurance (10^{12} cycles) [2], sub-nanosecond switching speeds [3], sub-10uA switching current [4], and large nonlinear current-voltage relation [5] and demonstrated operation in 10x10 nm devices [6]. All of these metrics are for research devices, not integrated with a CMOS process. In fact, two of the significant hurdles to overcome with ReRAM technology are integrating high performance ReRAM devices with a CMOS back end of line (BEOL) materials and processes and eliminating the high voltage electroforming step. This work reports initial results from the integration of a TiN/Ta/TaO_x/TiN CMOS compatible ReRAM structure. These initial results demonstrate that a CMOS integrated process which does not require a high voltage forming step and already exhibits performance on par with flash memory.

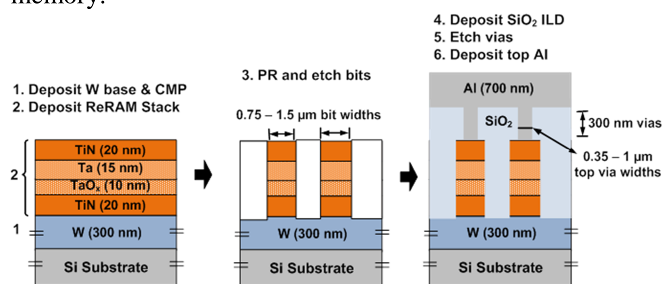
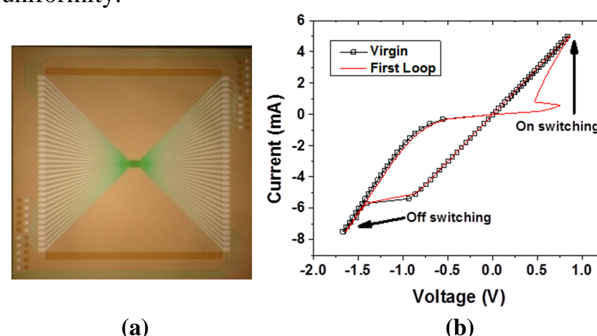


Fig. 1: Schematic illustration of the BEOL process used to create the TaO_x ReRAM structures.

The details of the fabrication process are illustrated schematically in Fig. 1. This is a "short loop" process used to evaluate process parameters, and is intentionally simplified from the full BEOL CMOS process which is being integrated with Sandia's in-house CMOS7 BEOL. The process begins with PVD deposition and CMP polishing of a 300 nm W layer on a standard p-type wafer. Next, the ReRAM stack is deposited using reactive PVD without breaking vacuum. The ReRAM stack consists of (top to bottom) TiN(30nm)/Ta(15nm)/TaO_x(5-15nm)/TiN(20nm). Experiments varying oxygen flow during the reactive PVD deposition of the TaOx allow optimization of switching behavior. Next, the ReRAM stack bits are dry etched with bit diameters of 0.75 to 1.5 µm, followed by the CVD deposition of the standard BEOL SiO_2 interlayer dielectric (ILD). The standard ILD SiO_2 recipe reaches 400°C and hence there was concern that the TaO_x film would be damaged. However results below indicate that the film was still functional. Finally, vias were etched above the bits with diameters ranging 0.35 to 1.5 µm. The best switching performance was obtained from the smallest via/bit combinations (0.35/0.75 µm). In this step, through vias were etched to contact the bottom metal (not shown in Fig. 1). Fig. 2(a) gives a photomicrograph of a final 32x32 crossbar produced from this process.

Basic current-voltage (I-V) characterization was performed on a probe station in a dark box, using an Agilent 4156C. I-V hysteresis loops were used as a method of initial characterization (Fig. 2(b)). The remarkable characteristic of Fig. 2 is that the virgin state is approximately equal to the ON-state of the device. During the initial sweep of the virgin device from +1.0 to -1.0 V, it is "electroformed" from the virgin ON state to OFF (SET) switching at approximately the same voltage as the subsequent OFF (RESET) switching cycles. In addition, the resistance of the subsequent ON state is also approximately the same as that of the virgin ON state. Hence, the device does not need an initial electrical precondition process (electroforming) involving high voltage and an irreversible resistance change, but simply switches off during the first negative cycle. The reason for this excellent result is a topic of investigation and may be related to specifics of the BEOL processes employed, such as the brief 400°C SiO_2 ILD deposition. This result is a major advancement in our CMOS integration work, as we no longer will require forming voltages above the capability of our logic transistors (3.3V), and is expected to lead to improved yield and device-to-device uniformity.



(a) **(b)**

Fig. 2: (a) Photomicrograph of the ReRAM crossbar die and (b) comparison of virgin and first I-V hysteresis.

Endurance was measured using an Agilent 81130A Pulse/Arbitrary Waveform Generator and an oscilloscope. An endurance of over 10^5 cycles was obtained, which is comparable with state of the art flash memory. CMOS compatible ReRAM processes generally exhibit lower endurance than individual devices. Present work indicates that this endurance can be improved by optimizing the process and electrical switching parameters.

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REFERENCES:

1. R. Waser et al., *Adv. Mater.* **21**, 2632 (2009).
2. M.-J. Lee, et al., *Nat. Mater.* **10**, 625 (2011).
3. C.T. Antonio et al., *Nanotechnology*, **22**, 485203 (2011).
4. F. Miao et al, *Adv. Mater.* **21**, 2632, (2011).
5. J.J. Yang et al, *Appl. Phys. Lett.* **100**, 113501 (2012).
6. B. Govoreanu et al., *IEDM Tech Dig., 31.6.2* (2011).