

A novel approach to clean surface for high mobility channel materials with in-situ Atomic Hydrogen Clean

Jeongwon Park*, Joe Griffith, Bo Zheng, Jerry Gelatos, Murali Narasimhan, Pravin K Narwankar

Applied Materials Inc., 3225 Oakmead Village Drive, Santa Clara, CA 95052, USA
E-mail: jeongwon_park@amat.com

Moore's Law on transistor scaling has impacted Si CMOS transistor density for the past decades. A number of non-silicon channel materials have been considered for advanced CMOS devices such as SiGe, Ge and GeSn (PMOS) as well as various III-V materials combinations including InGaAs and GaAs (NMOS). Ge/III-V channels on Si substrates are expected to be promising device structures for high performance CMOS in the future beyond the 10 nm technology node. Preparation of clean, atomically flat surfaces is an critical first stage in making a better interface contact area in semiconductor fabrication. This paper discusses a new cleaning technology on future channel materials (Ge/III-V) using a thermal atomic hydrogen source. This technique has several advantages over conventional wet, thermal, or plasma cleaning such as lower temperatures, no surface damage, less impurities, selective removal, and large area scalability. This study provides an effective method of uniform surface cleaning using a thermal hot wire atomic hydrogen source for next generation semiconductor fabrication processes beyond 10nm node with scalability to 450mm wafer size. In addition, this work offers a description of a new type of source design for use in the surface treatment of atomic hydrogen.

Since the interfaces require clean surfaces without damaging materials, it is an important parameter to generate high efficiency atomic hydrogen. As shown in Figs. 1 and 2, the etch rates with carbon based APFx films were measured to examine the cracking efficiency of molecular hydrogen with various process conditions. The surface area of wires plays a key role in increasing efficiency of H radical generation. The cracking efficiency of hydrogen gas (indicated by higher APFx etch rate) increases with increasing filament temperatures (Fig.1), and it is saturated with process pressure and H₂ gas flow (Fig. 2).

The metal contamination from the source is a critical criterion for evaluating this process for use in semiconductor manufacturing. The metal level measured by ICPMS promises to meet the current requirements (below 5X10⁻⁹ atoms/ cm²) for the semiconductor applications at various process conditions. SIMS/HRTEM performed at the interface indicated oxide layers at the interface for unclean sample; while a clear reduction (two orders of magnitude) in the O peak was observed with thermal hot wire atomic hydrogen on GaAs samples (See Fig.3) and on Ge (See Fig.4). In addition, cross-sectional TEM images show clean surface without physical damage on the top surface after atomic hydrogen cleaning process using thermal atomic hydrogen. The electrical contact resistance measurement was done on a diode structure (TiN (100nm)/1E19 /cm3 n+ Ge (150nm)/1E19 /cm3 p+ Ge (150nm)/i-Ge (700nm)/p-Si). Atomic hydrogen clean was shown to reduce the specific contact resistivity on n-Ge due to the reduction of the germanium oxide (GeOx), and surface passivation at the interface by H atoms. This study demonstrates a method to clean Ge and III-V, and reduced specific contact resistance (2.7x10⁻⁵ Ω-cm²) [1] using thermal atomic hydrogen cleaning process.

In summary, this study demonstrates a method of surface cleaning on Ge/III-V channel using thermal atomic hydrogen source, which will be a good candidate

technology for the future non-Si CMOS technology beyond 10nm node with scalability to 450mm wafer size. This system can be used not only for cleaning, but also for deposition of metal, dielectric, or composite thin films, or other applications.

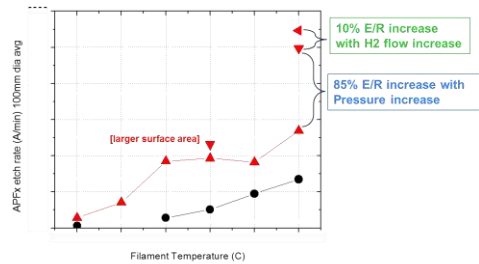


Fig 1. APFx etch rate as a function of filament temperature showing hydrogen radical efficiency indirectly.

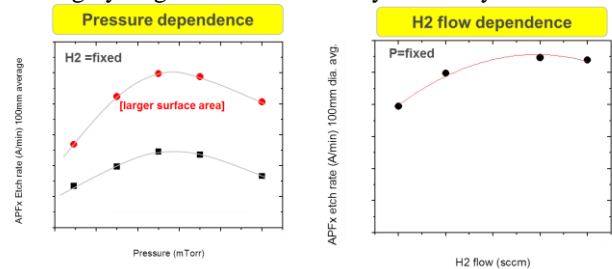


Fig 2. APFx etch rate as a function of pressure and H₂ flow at a constant filament temperature

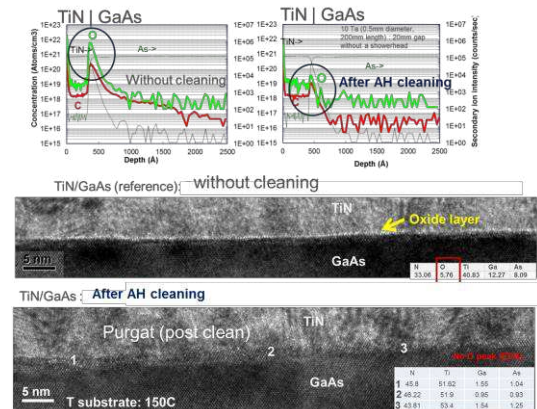


Fig 3. SIMS and TEM image of GaAs with TiN capping layer (100nm) pre and post atomic hydrogen treatment.

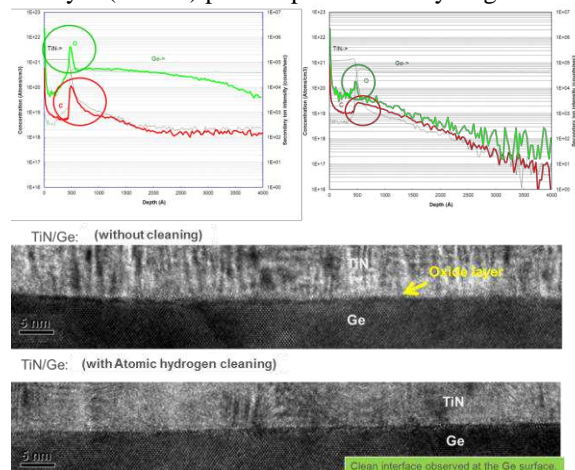


Fig 4. SIMS and TEM image of n-Ge with TiN capping layer (100nm) pre and post atomic hydrogen treatment.

[1] Ashish Agrawal, Jeongwon Park, Dheeraj Mohata, Khaled Ahmed and Suman Datta1, DRC 2012 (2012)