Abstract #2108, 224th ECS Meeting, © 2013 The Electrochemical Society

FEOL and BEOL Cleaning Challenges for 2x and sub-20 nm Technology Nodes

Akshey Sehgal
GLOBALFOUNDRIES
400 Stonebreak Road Extension
Malta, NY 12020

Aggressive scaling to 2x and sub-20 nm nodes has driven challenging particle and metal contamination requirements while introducing what was previously BEOL wet cleans into FEOL. So apart from the usual FEOL cleaning challenges, 2x and sub-20 nm node cleaning now include cleaning metal gates and exposed SiGe layers where the Ge is lost during conventional cleans (Ge has a tendency to oxidize and form water soluble GeO_2). In sub 20 nm technologies, FinFET cleans have to be performed while retaining the Fin profile with no stiction and removing residues from recessed areas as well. Wet cleans and cleaning approaches for these FEOL issues will be presented and discussed in the presentation.

For advanced technologies BEOL patterning schemes, titanium nitride (TiN) is widely used as a metal hard mask film protecting the inter-level dielectric (ILD) before metal or plating seed layer deposition steps. A wet etch is used to remove the residues formed during the ILD dry-etch step, and at the same time is required to remove some or all of the exposed TiN. The TiN metal hard mask is an enabling clean as it reduces the stack aspect ratio to improve the metallization process window & enables extending PVD Liner options. However, the clean must be accomplished with no undercut of the exposed stack and/ or bowing and no attack of exposed metal (Cu for Via 1 and higher metal layers or W for Via 0) at the bottom of the via. In addition the metal liner materials such as Ta, Ti, TaN and TiN need to be compatible with the TiN removal chemistry as well. The cleaning approach developed removed the TiN metal hard mask at the top of the stack but did not attack the TiN glue layer in the Via 0 liner. Results from this work will be presented as well.

TSVs, which allow the co-integration of various components such as RF, logic, memory, sensors by direct chip to chip stacking, are needed for mobile applications and drive the development of 3D stacking technology. High aspect ratio TSVs were implemented in an existing 20 nm Test Vehicle (TV). Etching of the TSV resulted in generation of sidewall polymer (SWP) and scallop formation on the TSV sidewall; these scallops pose a risk for leakage currents and stress points. The post TSV etch clean needs to remove the SWP completely despite the presence of the scallops and prepare the TSV surface for liner deposition. Post TSV clean results and the electrical results of sea of TSV arrays will be presented as well.