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Optimized Contact Engineering to Maximize Cell Current in NAND Flash Memory Technology

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In this research we have confirmed that Nand flash cell current increases by optimization of contact barrier metal(BM) deposition and plug implantation(IIP) doping condition, which result in improved contact resistance(Rc) and cell leakage. Plug IIP dopant, BF_2, which has been applied to P-type Transistor (TR) for lowering Rc sacrifices contact process margin in cell area of n-type occurred by cell leakage. We could dramatically improve P-type Contact Rc and contact process margin by lowering BM deposition process temperature and adopting plug IIP doping with phosphorous (Ph.) respectively.

As devices scale down, the problem of increasing Rc has been solved by BM optimization of Ti/TiN condition for stabilizing the interface between W contact and Si substrate [1]. Common contact process for N-type and P-type has been the limiting factor, because it caused P+ Rc increase issue due to the rapid diffusion of P+ boron throughout the following heat budget processes [2.3]. The increase of P+ Rc in sub 50nm Nand Flash eventually results in cell leakage issue by the lack of contact process margin and compensated N- cell area even though BF_2 is applied as contact plug IIP dopant. Figure 1 is a conventional Nand flash cell structure. It shows that as direct contact (DC) in plug IIP dopant BF_2 area gets too closer to N-LDD, it has higher possibility of compensating P- and N-. And as contact mis-align (M/A) occurs more, contact process margin gets narrower due to weakened cell leakage. Figure 2 indicates low temperature BM induces stable decrease in N+, P+, and Cell N+ Rc with small amount of heat budget according to BM deposition temperature, and different plug IIP dopant. Especially Ph. dopant condition decreases cell N+ Rc by 50% comparing to BF_2, so it is expected to improve cell operation margin in the coming device scaling down age. Figure 3 is the result of confirming contact process margin of each contact condition by intentional DC photo M/A in the cell N+ area. The Worst On Cell Current (WOC) is measured for the string with all programmed cells except the last one in the cell [4]. In (a), (b) with BF_2 applied cases cell leakage occurs and cell current decreases dramatically at 10 nm of DC M/A in high temperature BM condition and at that of 15nm in low temperature BM condition. Through the compensation between P- of BF_2 and the mis-aligned N- area cell leakage occurs in the PPW direction. (c) of Ph. application acquires stable WOC without cell leakage when DC M/A happens up to 30nm..

In conclusion increase in contact resistance and cell DC leakage issue can be solved by low temperature BM stabilizing P+ Rc and the best suitable plug IIP dopant condition same as N-type contact. Therefore, we have acquired contact process mis-align margin by 30nm per side, and improved cell current with better cell leakage.

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[2] H. S. Park et al., VLSI Tech., Systems, and Applications, (2001) 93
[3] S. B. Kang et al., IEEE, Interconnect Tech. Conf., (2000) 70.
[4] H. S. Oh et al., IEEE, Non-Volatile Memory Technology Symposium, (2005) 3

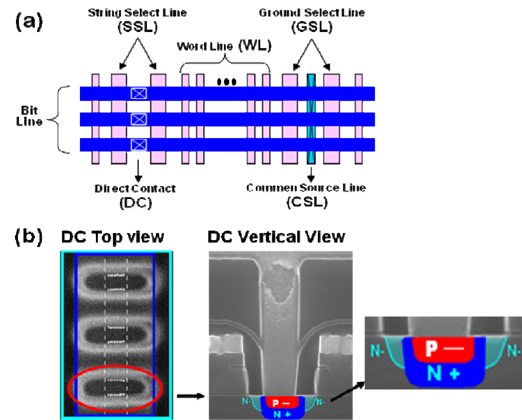

Figure1. (a) Nand Flash Cell String Structure. (b) Cell DC Contact Structure & Junction.

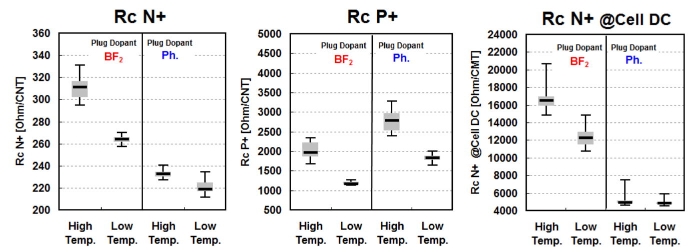

Figure2. N+, P+, Cell N+ Contact Rc as BM & Plug IIP Dopants.

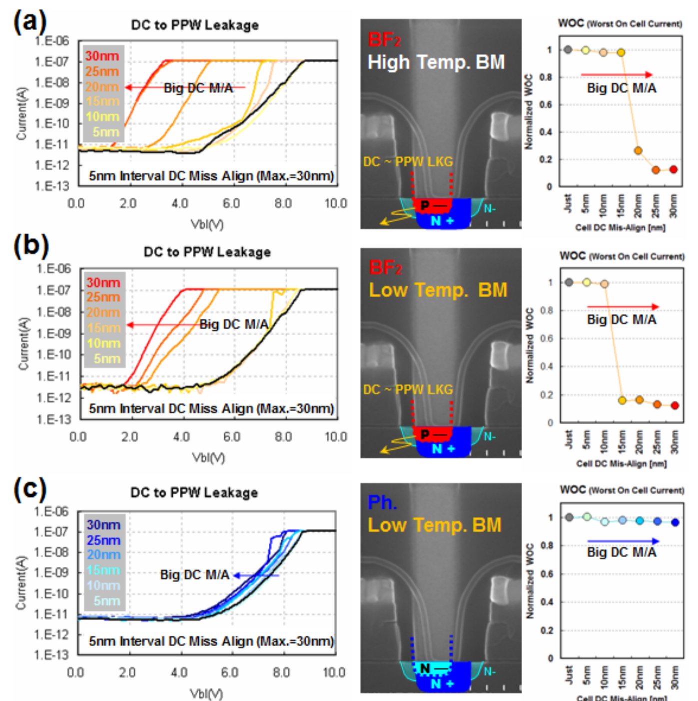

Figure2. Cell Leakage & Cell Current as Cell DC M/A (a) High BM & Plug IIP BF_2, (b) Low BM & Plug IIP BF_2, (c) Low BM & Plug IIP Ph.