# Vertical III-V nanowire-channels on Si

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Mature Si complementary metal-oxide-semiconductor (CMOS) technologies are encouraged to change their gate-architecture, channel material, and transport mechanism to avoid inherent limitations in transistor scaling for high-speed and low-power large scale integrated circuits (LSI). Field-effect transistors (FETs) with lower leakage current and steep subthreshold-slope (SS) are required for reducing the power consumption of the LSI. Our goals are to replace Si-channel by III-V nanowires (NWs), and the transport mechanism by tunneling transport. However, there are significant challenges in terms of epitaxy, device process. Here we report recent advances in integration of III-V NWs on Si and FET applications.

Recent advances in hetereopitaxial techniques, such as selective-area growth (SAG) have enabled integration of III-V NWs with Si substrates regardless of mismatches in lattice constant, thermal expansion coefficient, and polarity. We further developed these techniques for aligning vertical InGaAs NWs [1,2]. Fig. 1(a) shows a typical growth result of the InGaAs NWs on Si(111). Vertically aligned InGaAs NWs were grown on Si(111).

Next, we fabricated vertical surrounding-gate FETs (SGTs) using InGaAs NWs on Si as illustrated in Fig. 1(b). The device process is same as previous report [3,4]. The gate length ($L_G$) is 150 nm and gate-drain length ($L_{G\text{-}D}$) is 50 nm. The gate-oxide is $Hf_{0.8}Al_{0.2}O$ with a thickness of 7.0 nm (EOT = 1.30 nm). Fig. 2 (a) and (b) exhibit the output and transfer characteristic of the InGaAs CMS NW-SGT. The switching behavior shows n-type enhancement mode (normally-off) behavior. In this case, the nanowire is composed of InGaAs/InP/InAlAs/δ-doped layer/InAlAs/InGaAs core-multishell (CMS) NW as shown in Fig. 3. EDX-mapping shows very uniform modulation-dope layers were formed around the NW-sidewalls and Al segregation form barrier layers at the corner of the NW. This barrier layer splits the cylindrical HEMT layer to six-sided HEMT layer. The device shows the $I_{ON}/I_{OFF}$ was $10^6$, and a minimum SS was 70 mV/dec in Fig. 2. The $I_{OFF}$ was effectively reduced as compared to InGaAs NW. High tranceconductance ($G_m$) was obtained, 1.20 mS/μm at $V_{DS}$ of 0.50 V.

Beside the high performance vertical FET using the InGaAs NW-channel on Si, heterointerface across InGaAs NW/Si works tunnel junction for a tunnel FET. Fig. 4 (a) exhibits illustration of the device structure and Fig. 4(b) shows transfer characteristic of the fabricated InGaAs NW/Si TFET at drain-source voltage ($V_{DS}$) of 0.01 – 1.00 V. Switching behavior with a SS of 80 mV/dec was observed under reverse bias direction ($V_G$ is positive for *n-i-p* junction). This switching characterization appeared at the $V_{DS}$ of 0.05 V. Also, the SS became slightly steeper with increasing the $V_{DS}$. Under low $V_G$ in Fig. 4(b), steep SS region observed whose minimum subthreshold slope under 60 mV/dec. Further scaling such as NW-diameter and EOT is required for maintaining the steeper SS region under higher $V_{DS}$ and $V_G$ bias condition.

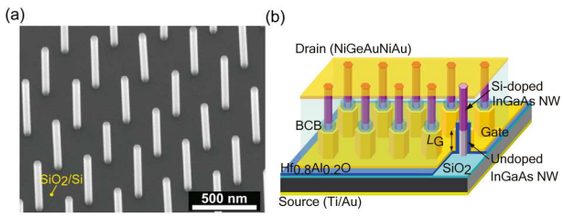


**Fig. 1**(a) SEM image showing representative growth result of InGaAs NW on Si by selective-area growth. (b) Illustration of surrounding-gate FET using vertical FETs on Si.

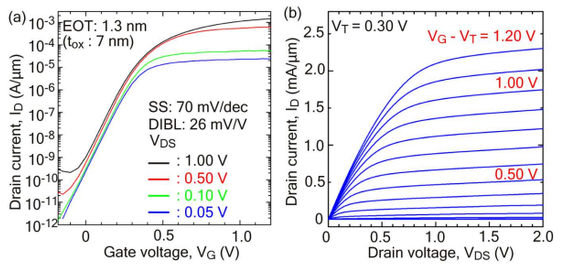


**Fig. 2.** (a) Output characteristic for InGaAs CMS NW-SGT on Si substrate, (b) transfer characteristic

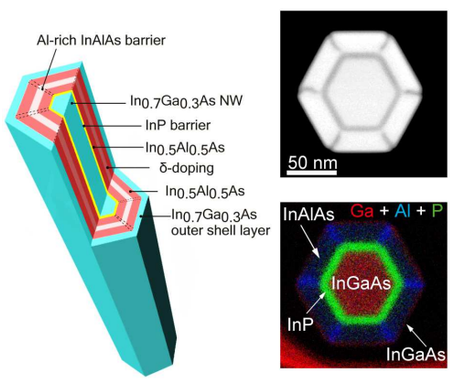


**Fig. 3**. Illustration of InGaAs CMS NW with HEMT structure and HAADF-STEM, EDX mapping of the cross section.

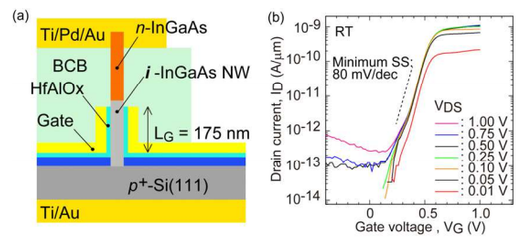


**Fig. 4.** (a)Device schematics of tunnel FET using InGaAs NW/Si heterojunction, (b) Output characteristic.

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