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Characterization of Local Stress in Silicon around Through-Silicon Via Interconnects by Using micro Raman Spectroscopy

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TSV (Through Silicon Via) is one of the key elements for emerging 3D integrated silicon devices with high bandwidth interconnections. However, the incorporation of TSVs with copper plating process poses a significant challenge to device reliability due to the thermal stress distribution in Si that arises due to the mismatch in the coefficient of thermal expansion mismatch between Cu and Si. The varying thermal stresses as a function of position away from the TSV can result in carrier mobility variance as well as failure of the integrated TSV structures though Cu extrusion, crack, and delaminations. In this study, the effect of the TSV size on the overall stress distribution in Si was evaluated using micro Raman spectroscopy and the experimental results were compared to the finite element simulations (Technology Computer-Aided Design, TCAD) of the TSVs. The TSVs with and without the overlayers from the back end of line (BEOL) process were studied to understand the stress development in the real device configurations. Micro Raman spectroscopy revealed that the compressive out-of-plane strain increases with Cu via size, and the trend is consistent with the TCAD simulations. The results from the present study suggest that micro-Raman spectroscopy is a viable approach to characterize the local stresses in the integrated TSV structures that can be easily incorporated in line production.