Conductive Bridging Random Access Memory Cell Fabricated with Top Ag Electrode, Polyethylene Oxide Layer, and Bottom Pt Electrode

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There are two types of ReRAM cells, unipolar and bipolar switching ReRAM, depending on the insulator material property [1]. In particular, many researchers have been interested in conductive-bridging random-access memory (CBRAM), which shows a bipolar switching ReRAM characteristic [2]. However, their nonvolatile memory characteristics, such as retention time and program/erase cycles, should be improved further to achieve commercial-level nonvolatile memory-cells. In our study, we developed a CBRAM cell fabricated with a sandwich structure of a reactive Ag electrode, polymer electrolyte (polyethylene oxide: PEO), and inert Pt electrode and investigated their nonvolatile memory characteristics, such as the bi-stable current-density verse voltage (*I-V*) curve, retention time, and program/erase cycles. In addition, we investigated the dependency of nonvolatile memory characteristics on the weight percentage of PEO in detail. Arrays of 20 × 20 CBRAM cells were fabricated on SiO_2 film grown on a silicon wafer, as shown in Fig. 1. Arrays of 20 × 20 nano-holes with 250-nm in diameter were pattered on the bottom 50-nm-thick Pt-electrode by using lithography and etching, where the thickness of the SiO_2 film, which isolated the holes, was 50 nm. Then, PEO was spin-coated on the hole arrays at 2000 rpm for 120 s and was baked at 60°C for 5 min. Note that the PEO was mixed with a co-solvent of acetonitrile and ethanol at 30°C for 3 hrs. Afterward, top Ag electrodes 300-μm in diameter and 200-nm in thickness were thermally evaporated at an evaporation rate of 1.0 Å/s under 10^{-5} Pa by using a shadow mask. Thus, the CBRAM cells have a sandwich structure of a bottom Pt electrode, PEO, and top Ag electrode. For the CBRAM cell with 0.3 wt% PEO, after a forming process, it showed the typical ReRAM characteristic of having a set voltage (V_{set}) of 0.54 V, a low resistance state (LRS) of 2×10^4 A·cm^{-2}, a reset voltage (V_{reset}) of -2.62 V, and a high resistance state (HRS) of ~1×10^1 A·cm^{-2} when the bias was scanned from 0, 5, 0, -5, and 0 V, as shown in the left figure of Fig. 2 (a). Thus, a CBRAM cell could operate with nonvolatile memory behavior when the current density (I_{on} or I_{off}) was read at 0.5 V after applying the above V_{set} (programming) or V_{reset} (erasing), as shown in the center figure of Fig. 2 (a). For the CBRAM cell with 0.4 wt% PEO, the *I-V* curve showed the typical bipolar switching characteristic of a CBRAM cell, where V_{set} and V_{reset} were 0.58 and –2.56 V, respectively, as shown in the left figure of Fig. 2 (b). A retention time of 1.0×10^5 s was obtained by sustaining a memory margin (I_{on}/I_{off}) of 1.0×10^4, a sufficient level for commercial memory cells, as shown in the center figure of Fig. 2 (b). Program and erase cycles of 10^3 was obtained by sustaining a memory margin (I_{on}/I_{off}) of 1.3×10^4, which demonstrated the best nonvolatile memory characteristics among the various PEO wt%, as shown in the right figure of Fig. 2 (b). For the CBRAM cell with 0.8 wt% PEO, the *I-V* curve did not show the typical bipolar switching characteristic of a CBRAM, where the absolute V_{reset} (–0.16 V) was much less than the absolute V_{set} (1.88 V), as shown in the left figure of Fig. 2 (c). A retention time of ~1.0×10^4 s was obtained by sustaining a memory margin (I_{on}/I_{off}) of 3.2×10^2, as shown in the center figure of Fig. 2 (c). Program and erase cycles of less than 5×10^2 were obtained by sustaining a memory margin (I_{on}/I_{off}) of 2.6×10^2, as shown in the right figure of Fig. 2 (c). In particular, the longest retention time with the maximum memory margin was obtained at 0.4 wt%. The dependency of program and erase cycles on the PEO wt% for CBRAM cells showed that the longest program/erase cycles with the maximum memory margin were obtained at 0.4 wt%.

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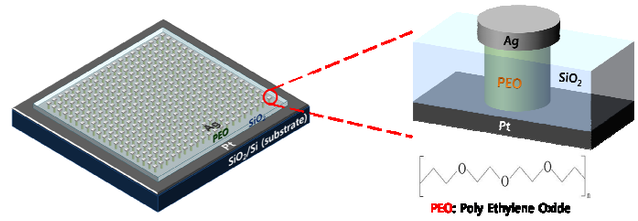

Fig. 1. Schematic structure of conductive-bridging random-access memory cells fabricated with sandwich structure of top Ag electrode, polyethylene oxide (PEO) layer, and bottom Pt electrode on 250-nm hole patterns.

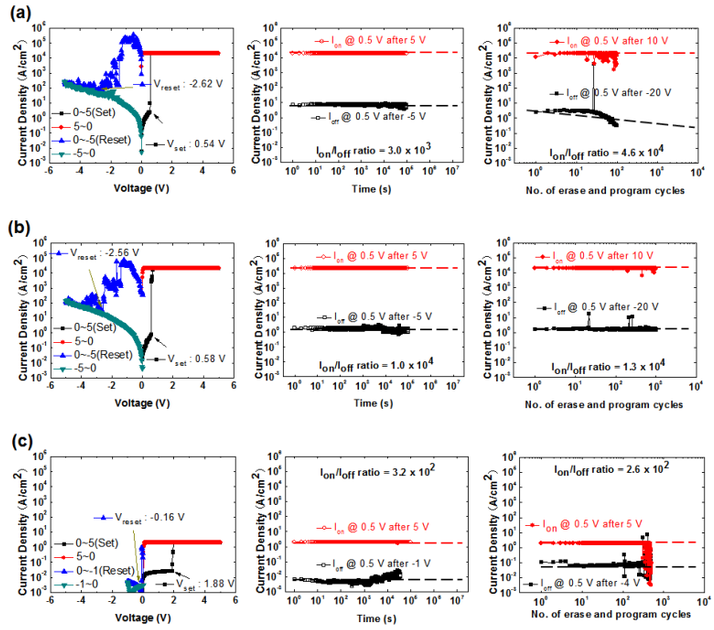

Fig. 2. Dependency of nonvolatile memory characteristics such as current density vs. voltage, retention time, and program/erase cycles on PEO wt %: (a) 0.3, (b) 0.4, and (c) 0.8 wt%

Reference

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