Extremely Short Channel Si-MOSFETs Prepared on SOI Substrates Using Anisotropic Wet Etching

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Studies of nanometer-scale Si-MOSFETs are increasingly important in order to look ahead the scaling limit of industrial CMOS technology. This work presents our experiments of extremely short channel MOSFETs, as short as 3 nm, approached by V-groove formation on SOI using an anisotropic wet etching technique [1, 2].

Starting from (001)-oriented 80-nm-thick SOI layer, V-grooves were engraved by anisotropic etching nature of tetramethylammonium hydroxide (TMAH) solution. The gate stack consists of HfO_2 dielectric film with SiO_2 interface layer and TaN/poly-Si electrode films. Following to the gate patterning, ion implantation was processed, BF_2^+ at 15 kV and $2\times10^{15}/cm^2$ for p-FETs and P^+ at 15 kV and $2\times10^{15}/cm^2$ for n-FETs, respectively. Activation and diffusion of dopants was promoted by annealing at 1000°C for 10 min. The devices were finally metallized and annealed in H_2 gas at 400 °C for 30 min.

Cross-sectional TEM image of the V-groove MOSFET is shown in **Fig. 1**. The V-groove consists of atomically flat Si(111) facets. The channel thickness below the V-grooves is as thin as 1 nm. The channel length, determined by the width of V-groove bottom is as short as 3 nm. It is noted that the SOI layer is uniformly doped with high concentration dopants by the long-period anneal at 1000°C. The MOSFET thus fabricated is the junctionless-FET (JL-FET) [3]. The current flow is controlled at the ultrathin channel region with 3-nm-length and 1-nm-thickness. The thick S/D region contributes to the reduction of parasitic resistance.

The electrical characteristics MOSFETs with 3.2 nm EOT and 1.5 nm EOT are shown in **Fig. 2**. Performances of FETs with 3.2 nm EOT are normally on. This is the nature of JL-FETs. It turns to be normally off when the EOT is scaled to 1.5nm. Threshold voltages for both n-FET and p-FET are optimal for low-power operation of CMOS circuits. It can be seen that EOT scaling does not increase the maximum drive current. This is because the drive current in JL-FETs is simply determined by the resistance of the channel. Anyway, EOT scaling is a critical technology for the extremely scaled MOSFETs.

Several quantum effects are known to become dominant when the typical dimensions of Si structures are reduced to be less than 10 nm. Source-to-drain tunneling [4] degrades the performances of short channel MOSFETs. On the other hand, expansion of band gap [5] and reduction of dielectric constant [6] in ultrathin Si films are expected to enhance the device performance. Furthermore, inactivation of dopants due to dielectric confinement effect [7] helps to control the channel potential by the gate bias voltage. At the ultrathin channel region shown in Fig. 1(b), competitive action of these quantum effects is likely to responsible for the superior modulation of current flow.

Acknowledgements

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References

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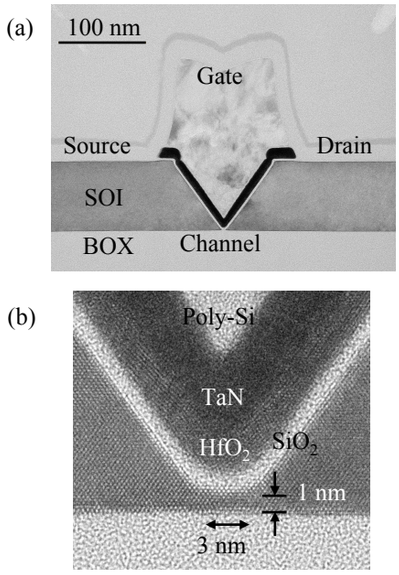

Fig. 1 (a) TEM image of the V-groove MOSFET and (b) the high resolution image of the channel region.

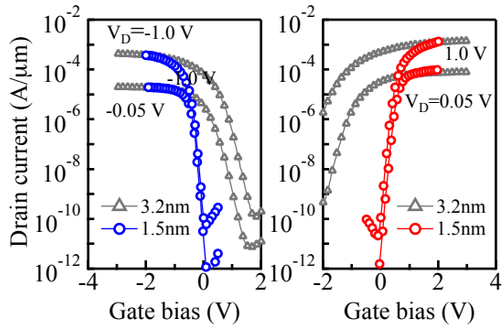

Fig. 2 I_D-V_G characteristics of p-type (left) and n-type (right) V-groove MOSFETs with 3.2 nm EOT (triangles) and 1.5 nm EOT (circles).