Copper Seed Layer Wet Etching for 3D Integration

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Advanced packaging is a hot topic more and more investigated to improve 3D Integration. In this context, applications are numerous, going from interposer to packaging (wafer to wafer stacking and die bonding report)[1]. For those applications, ranging from Redistribution Layer (RDL) level, to solder joints also called solder bumps or copper pillars, a wide type of electroplated materials is used (as diverse as Cu, Ni, Au, SnAg, alone or combined to each other [2]). All these integration cases commonly use Cu deposited by Physical Vapor Deposition as the seed layer for ElectroChemical Deposition. Even if different barrier layers are studied depending on the applications, Cu seed layers remain the key process. After ECD growth and mask stripping a critical process step is mandatory to achieve seed and barrier layers removal. Regarding current dimensions and cost of ownership, the process of record for Cu seed layer etching is still the wet process. RDL critical dimensions can be as small as 8µm while thicknesses vary in the range from 1.5µm to 10µm. On the other hand solder joints are sized from 15µm to 100µm combined with thicknesses from 4µm to 80µm.

In this paper, Cu wet etching processes are investigated both on 200mm and 300mm wafers. Chemical mixture widely used is a mix of sulfuric acid and hydrogen peroxide diluted in DI Water (mixture called DSP). First, Cu wet etch kinetics are investigated either in immersion mode on wet bench or on single wafer spin-on tool (SWT) on Cu PVD blanket wafers. As expected etch rate recorded with a SWT is drastically higher than using manual immersion mode (Figure 1). While the gravity dispense of the spin-on tool increases the ER by a factor 4 compared to immersion mode, the combination of spin-on with a spray dispense allows to reach a factor 7. This behavior confirms both the need to evacuate by-products but above all the necessity to renew active species as close as possible from the reaction interface as spray mode facilitates transfer through the boundary layer. Nevertheless the fastest kinetic on blanket wafers can't be considered as "the true life" on patterned wafers as the aim of the process is to find a compromise between total Cu seed layer removal and controlled undercut. Lateral etch when ECD copper is embedded is also critical. ECD Cu wet etch is thus studied on RDL wafers in order to predict dimensions after wet etch (Figure 2). ECD Cu etch is faster than PVD Cu etch with a factor of approximately 2.5 due to structure difference (ECD Cu is not annealed). Higher speed rotation seems to reduce top ECD consumption whereas laterally consumption is the same. As a matter of fact, the time to totally remove the seed layer is critical for small dimensions [3]. On this way the pattern density is also a parameter influencing Cu wet etch as high density area needs an over etch from 10 to 50% depending on different structures studied.

Most of the time the DSP mixture works well whatever the different ECD stacks (from ECD Cu alone or ECD Ni/Au or ECD Cu/Ni/Au) exposed during Cu seed removal. Despite this observation, the DSP Cu seed etch in presence of ECD Cu/SnAg or Cu/SnAgCu can randomly reveal specific defects which can, in the worst case, compromise the reflow step required for solder bump reshape (Figure 3). Numerous parameters were investigated through the flow including lithography, ECD growth, stripping and wet etching. The defects appearance was linked to the sulfuric acid. After investigation, the replacement of sulfuric acid by phosphoric acid definitively fixes the defect issue whatever the chemical dispense mode. As a new process with phosphoric acid is implemented, the new mixture kinetic is studied. In parallel, different characterizations are conducted in order to find the root cause of the defects revealed on SnAg with sulfuric acide: SEM, EDX, FIB, TEM-EELS, µAuger.

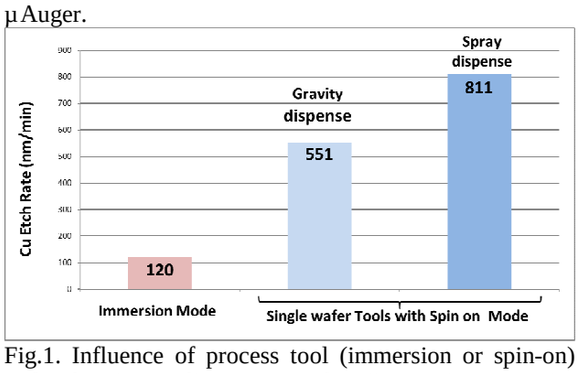


Fig.1. Influence of process tool (immersion or spin-on) and chemistry dispense mode (immersion, gravity dispense and spray) on copper wet etch rate for DSP 1/1/100 (H_2SO_4/H_2O_2/EDI) mixture.

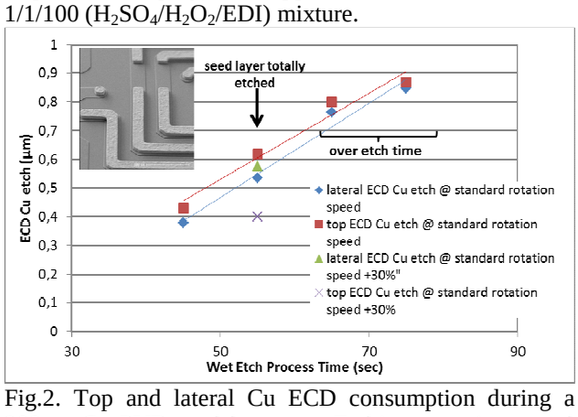
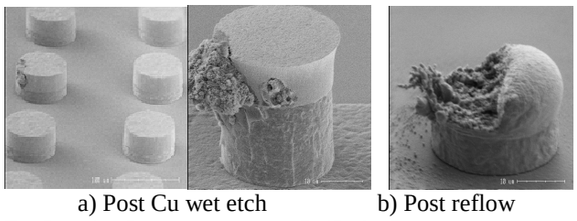


Fig.2. Top and lateral Cu ECD consumption during a 200nm Cu PVD seed layer wet Etching on spin-on tool for RDL configuration.



a) Post Cu wet etch b) Post reflow

Fig.3. a) Solder bumps Cu/SnAgCu with random defectivity after seed layer wet etch with sulfuric acid and b) impact post reflow step.

References

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