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ULTRA-NARROW, HIGH ASPECT RATIO TRENCHES FOR USE IN MINIATURIZED POLY-SIGE ACCELEROMETERS

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This paper reports the realization of high aspect ratio trenches (25:1) in a 4µm thick poly SiGe layer at a temperature budget ≤ 450^0C. By combining deep ultraviolet (DUV) lithography, deep dry etching with a silicon dioxide (Si-oxide) hard mask and a gap narrowing process [1], trench widths as narrow as 150nm can be realized. The achieved results demonstrate significant (~20x [2]) improvement of the narrow trench aspect ratio for miniaturized MEMS accelerometers, and a nearly uniform gap throughout the trench depth. An undercut to mask opening ratio of 0.03 was realized, which is ~10 times better than values recently published [3]. Similar results have only been achieved with a gap reduction process [4] that requires a temperature of 1000^0C [4], which cannot be used for an above-CMOS MEMS process.

This high aspect ratio, narrow trench process was developed for a poly-SiGe layer, deposited at a temperature of ~450°C, which can be used as the structural layer of above-CMOS monolithically integrated lateral capacitive accelerometers . Having narrow sensing gaps between the comb fingers enables the miniaturization of the accelerometers without sacrificing their sensitivity.

Indeed, reducing the overall dimensions of an accelerometer is expected to lead to a lower sensitivity S due to the decrease in mass m [5]:

$$S= (2\varepsilon Am)/(kdo^2)$$

where A is the overlap area of the successive fingers, k is the spring constant and d_0 is the sensing gap. Clearly, by developing narrow gaps, and thus lowering d_0, this drawback can be overcome [2].

The SiGe MEMS technology used in this work consists of a 400nm thick bottom electrode layer, a 3µm thick sacrificial Si-oxide layer and a 4µm thick SiGe structural layer (Figure 1). The poly-SiGe structural layer is deposited by using a combination of chemical vapour deposition (CVD) and plasma enhanced CVD (PECVD) [6]. To realize the ultra-narrow trenches by DUV lithography, a 250nm thick Si-oxide hard mask is used in combination with a 250nm thick resist layer and a 50nm thick BARC (Bottom Anti-Reflective Coating) layer. Combining a 200nm resist opening with a sloped etch of the hard mask, results in a reduced opening on top of the SiGe structural layer of ~128nm (Figure 2). Next deep dry etching was performed by using the Bosch process. The passivation: etch time ratio was optimized to a value of 1.8 sec passivation: 1.4 sec etch. The etch depth and profile was evaluated after different number of etch cycles (Figure 3 and 4, Table 1). From these results the optimal number of cycles to complete the 4 µm thick layer etch was determined to be 70 (Figure 5). To have narrow trenches in the end, it is important to control the first undercut. This was realized by performing the passivation step before the etch step.

After the optimization of the etch profile, further reduction of the trench gap was enabled by a gap narrowing technique [1]. This technique consists of an additional conformal CVD SiGe deposition on the side walls of the trench in combination with a subsequent mask less dry etching of the SiGe layer deposited on the bottom of the trench (Figure 6). The time-defined etch back process uses HBr as the etchant gas. Detailed pictures of the side wall deposition and the result of the bottom SiGe etch for a 200nm trench are shown in Figure 7. This CVD-based gap narrowing process has many benefits. Apart from reducing the trench dimension (Table 2), it also reduces the first undercut of the Bosch process significantly. The results of the gap narrowing process for 300nm trench widths are shown in Figure 8 and Table 2.

In conclusion, we have demonstrated a process for creating ultra-narrow trenches in 4 µm thick poly-SiGe layers. The process is based on the narrowing of, initially ~250nm wide gaps after DUV lithography and etch, to ~150nm wide gaps by the use of a conformal deposition and etch back. This process has been successfully implemented to fabricate miniaturized SiGe based MEMS accelerometers (Figure 9).

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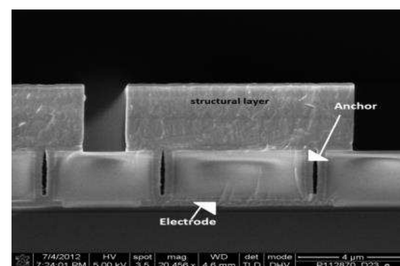

Figure 1:SiGe MEMS Technology

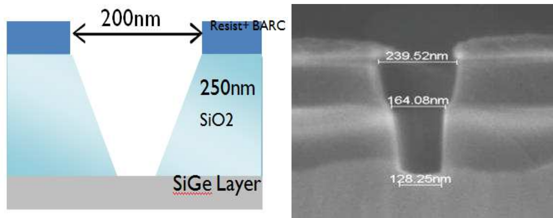

Figure 2: DUV litho print and hard mask opening

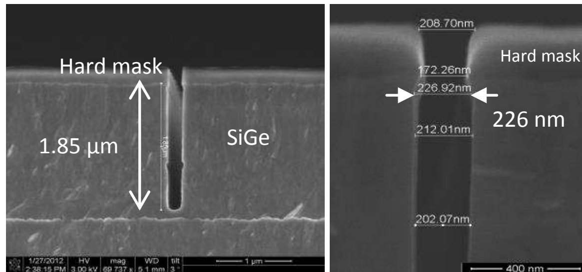

Figure 3: 22 cycles of etch

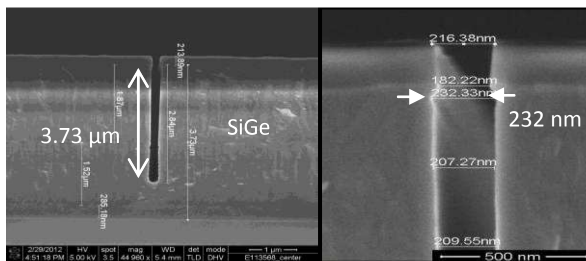

Figure 4: 50 cycles of etch

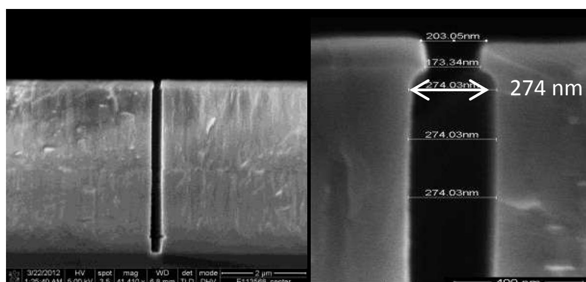

Figure 5: 70 cycles of etch

Table 1: Results of DRIE process:

DRIE parameter	Etch Cycles	Trench Depth (µm)	Undercut (nm)
Passivation	22	1.85	13
1.8 secs/Etch	50	3.73	16
1.4 secs	70	4	37

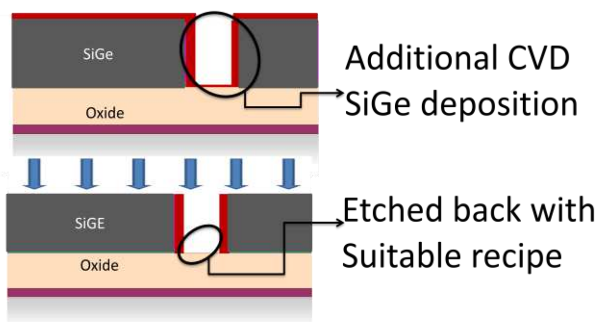

Figure 6: Schematic of the gap narrowing technique

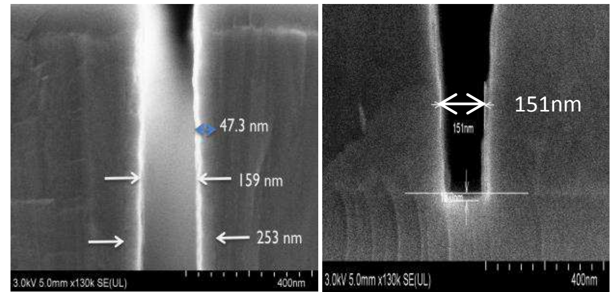

Figure 7: Conformal CVD deposition and etch back for 200nm mask opening

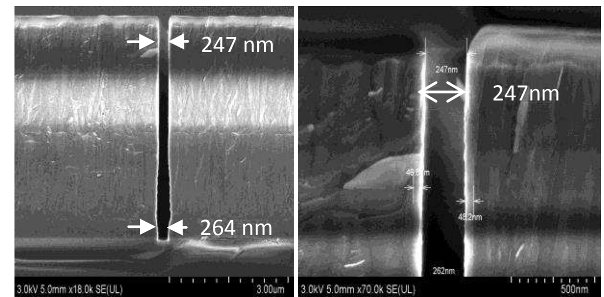

Figure 8: SEM of gap narrowing for 300 nm mask opening

Table 2: Results of gap narrowing for different gap

Mask opening (nm)	Trench width after DRIE (nm)	Trench width after gap narrowing (nm)		AR	Under cut (nm)	Under-cut /mask ope-ning
		Top	Bottom			
200	253	159	151	25	6	0.03
300	357	247	264	16	11	0.04

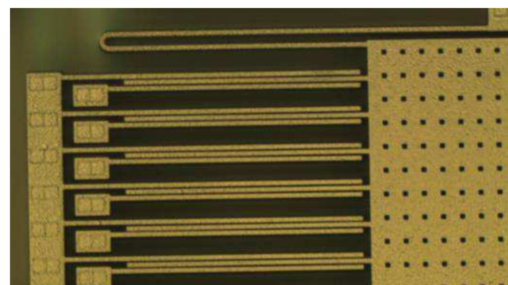

Figure 9: Optical image of a miniaturized accelerometer with gaps of 200nm.