Low temperature direct bonding 3D Stacking Technologies for high density device integration

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3D integration aims at providing highly integrated systems by vertically stacking and connecting various materials, technologies, and functional components together.

Direct bonding allows the vertical stacking of top and bottom layers for later process integration options. This stacking can be performed in; wafer-to-wafer (W2W) bonding or die-to wafer (D2W) bonding.

We will present here the creation of advanced substrate or stack for 3D integration by the Smart-Cut™ technique

Oxide bonding: this technique enables the 3D monolithic integration at the wafer level [1]or the stacking of two processed layers[2]. The temperature process is as low as 150°C and the oxide deposit can be monitored in order to highly increase the bonding energy [3].

Metal bonding: The bonding with Cu, W, Ti of plain metal layers has been demonstrated [4], fig 1.. Combined with thinning, patterning and etching this technique will enable the realization of non-volatile memory [5]

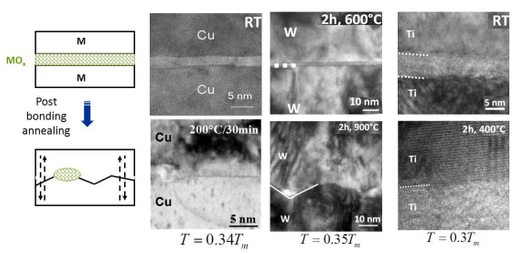

Fig 1 :TEM observation of the metal bonding interface. At room temperature each bonding interface present an thin metal oxide layer. At 0.3Tm the oxide layer is instable and is dissolved. The electrical behavior is perfect.

Smart cut and SPER: a way to thin the upper substrate down to tens of nm is to use the Smart Cut™ process which combines hydrogen implantation and bonding. Mainly used for SOI production is was recently demonstrated with metal bonding at low temperature [6]. In that case, to recover the upper silicon quality a solid phase epitaxial recristallization technique (SPER) was used. At process temperature as low as 500°C a vertical p/n junction was successfully transferred as shown by the I(V) curves obtained after transfer and SPER technique [7],fig. 2.

Metal /oxide patterned surface bonding: in that case the aim is to create the vertical interconnects at the bonding level.
Copper pad sizes varying from 5µm to 500µm with a pitch of 10 µm and 40µm were investigated and excellent

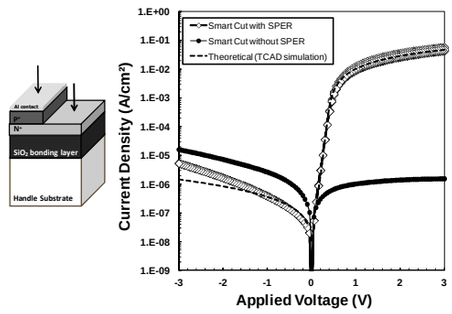

Fig 2. I(V) diode characteristics after Smart Cut™ layer transfer

bonding interface defectivity was demonstrated Fig. 3. Typically, various interfaces are formed after patterned Copper bonding. The highest bonding energy is obtained for Copper-Copper (Cu-Cu) interfaces, followed by SiO_2-SiO_2. The Cu-SiO_2 interface leads to the weakest adhesion even after 400°C annealing. Copper interdiffusion and/or grain growth across the Cu-Cu bonded interface are the driving forces for achieving high bond strength [8]. The achieved bonding strength has been sufficient to sustain post processes such as silicon back thinning using coarse and fine grinding. In terms of electrical characterization, a specific contact resistance of 0.5Ω.µm2 for 10x10 µm2 contact area after annealing at 200°C and 400°C for 2h was achieved [9]. The resistance per node extracted from a ~30K daisy chain after 400°C post bond anneal showed negligible resistance induced by bonding. In addition, initial reliability data based on Electromigration (EM) testing shows that the bonded metallic interfaces are not the dominant path for the EM phenomina.

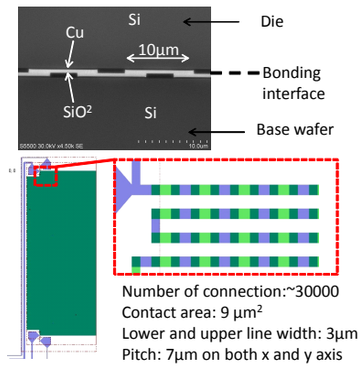

Fig 3: SEM observation of a copper daisy chain with a 7µm pitch.

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