Interrelationship between Defects and Electrical Characteristics/reliability Analyzed by Integrated Evaluation Platform for SiC

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Commercially available SiC wafers still include thousands of defects while the large defects, such as micro pipes, are almost eliminated. Large progress about reduction of the defects on both SiC wafers and epitaxial films has been made. For example, stacking fault (SF) and the other poly-type inclusions are minimized by the optimized step-flow epitaxial growth on the off-cut wafers which sometimes result in the rough surface with step-bunching. Fortunately, the epitaxial film with very flat surface (almost bunching free) is available these days.

It has been widely accepted that wide-band-gap semiconductor SiC can realize low-loss semiconductor transistors and diodes for the power electronics applications. In practice, we can get high-performance and fairly large-size (more than several mm square) power devices. We know that no device is fabricated without defects. For managing the SiC-device mass production, it is very important to evaluate interrelationship between the defects and the electrical characteristics/reliability.

We have put steady effort to establish the Integrated Evaluation Platform (IEP) for SiC wafers and epitaxial films.[1] Our IEP consists of the observation-recognition system (ORS), the defect-structure analyses (DSA), and the electrical-characteristics analyses (ECA). The ORS is based on the confocal microscope with differential interference contrast (SICA: Lasertec) featuring high-resolution surface image with <1um resolution. The ORS can recognize/classify/locate the defects. The DSA (TEM, SEM, AFM, PL, X-ray topography, etc.) are performed to elucidate the defect structure. The numerous ECA data using large numbers of small electrodes, each of which includes small number of defect (almost zero or one), provides simple information about relationship between defects and the electrical characteristics/reliability. For example, the time-dependent dielectric-breakdown (TDDB) under constant stress current of 0.15mA/cm2 were measured using hundreds of MOS capacitors with small 150um Al electrodes. .

The step-bunching on the relatively flat SiC epitaxial-film surface was carefully investigated by the ORS. It is discovered that the step-bunching partly distributes and consists of large numbers of crushed-flat triangle-shape defects stretching in a row along the scratches as shown in Fig.1.

Figure 2 shows the Weibull-distribution plot of the Q_{bd} derived by the TDDB. Two types of distributions of the Q_{bd} are observed as indicated by distribution1 (D1) and distribution2 (D2) in Fig. 2. The D1 exhibits narrow distribution at high value of Q_{bd} on the flat surface without step bunching. The D2 exhibits wider distribution at lower value of Q_{bd} than the D1. The Q_{bd} measured at the electrodes on the step bunching are among D2. Some large defects make the Q_{bd} very low while the other defects exhibit small effects.

IEP for SiC wafers and epitaxial films is established and provides information about the interrelationship between defects and electrical characteristics/reliability. As an example of the results, it is derived that SiC step-bunching defects on the epitaxial wafer partly distribute and degrade the Q_{bd} of the SiC-MOS.

Reference
[1] M. Kitabatake et al., Materials Science Forum, Vols. 740-742 (2013) p. 451

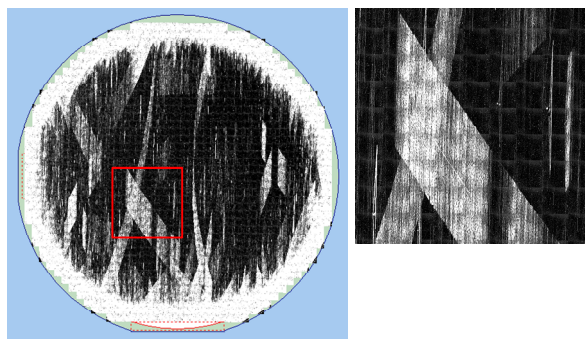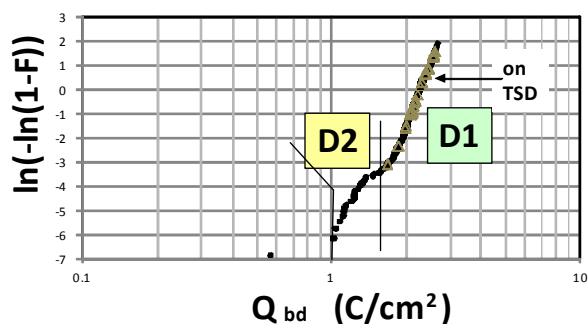Figure 1. Step-bunching map of 3 inch SiC epitaxial wafer and the enlarged image.

Figure 2. Weibull-distribution plot of the Q_{bd}.