

Impurity-induced Tin Incorporation during Copper Electrodeposition

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Abstract

Electroplated copper that is deposited in the presence of an additive package including an accelerator, a suppressor and a leveler is widely used in fabrication of interconnects in semiconductor manufacturing [1]. More recently, incorporation of a small amount, generally less than 1%, of a secondary metal element such as tin, indium or aluminum into copper interconnect structures has been shown to improve the device reliability and electromigration [2]. While studies are available on the electrodeposition of Cu alloys with other metals, these studies focus on codeposition of bulk alloys [3]. Due to the much more negative reversible potential of Sn, the co-deposition of Sn and Cu requires a higher current density than that normal used for pure Cu superfilling which disables the void-free filling.

In this study, the incorporation of Sn during Cu damascene plating was investigated at conditions that achieve void-free filling. The content of Sn in the Cu deposit is lower than 1% to avoid significant resistivity increase. The study focused on the effects of the additive package used, the current density, and the feature size on the tin incorporation.

Secondary ion mass spectrometry (SIMS) was used to analyze the low Sn concentration in Cu. In this study, the Sn concentration in Cu was found to increase with the non-metallic impurity levels. Because the plating chemistry and plating current have strong impacts on the incorporation of the non-metallic impurities, [4] they were also found to change the degree of Sn incorporation. For example, Cu films plated at a lower current density, which showed higher non-metallic impurity levels, were found to incorporate more Sn, opposite to the expectation from the more negative reversible potential of Sn [3]. In

addition, the Sn incorporation is also higher in narrow lines as compared with overburden films which correlates well to findings for non-metallic impurity levels [5, 6]. By combining a plating chemistry which results in high non-metallic impurity levels and a low current density void-free 40-nm wide Cu lines with up to about 0.1% Sn were plated, a 10-fold increase from the overburden film (Figure 1).

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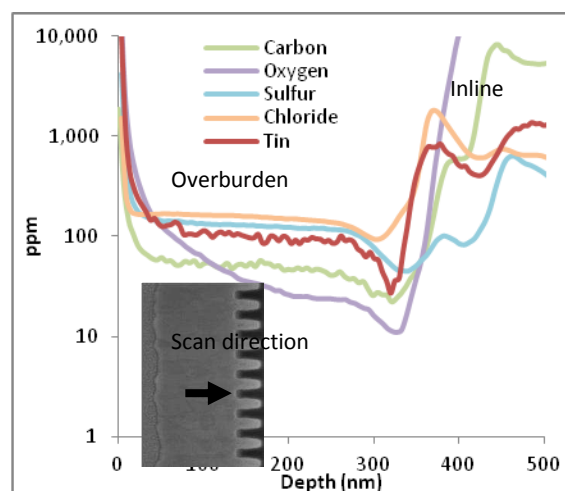


Figure 1. SIMS depth profiles of Sn, C, O, S, Cl in narrow Cu lines with overburden.

References

1. Andricacos, P.C., et al., IBM Journal of Research and Development. **42**(5), p. 567-574 (1998)
2. Gambino, J.P., 17th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, p 1-7 (2010)
3. Volov I, et al., Electrochimica Acta **89**, p. 792-797 (2012)
4. Huang Q., et al., Journal of the Electrochemical Society, **159**(9), p. D526-31 (2012)
5. Kelly, J., et al., Journal of the Electrochemical Society, **159**(10), p. D563-9 (2012)
6. Zhang W., et al., Journal of The Electrochemical Society, **152**(12), p. C832-7 (2005)