High Electron Mobility in Germanium Junctionless n-MOSFETs

S. Kabuyanagi, T. Nishimura, K. Nagashio and A. Toriumi
The University of Tokyo, JST-CREST
7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan

1. Introduction

Junction-less FET (JL-FET)[1] is gaining much attention for solving the problem of sharp doping profile formation and for improving the short-channel effects. Then, we have already demonstrated Ge p-channel JL-FET based on its high bulk mobility[2]. Meanwhile, it should be noted that the electron mobility in bulk n-Ge is one order higher than that in n-Si in heavily doped region ($N_D=10^{18}\sim10^{19}$ /cm^3)[3]. In this work, we demonstrate n-channel JL-FET fabricated on GeOI substrate.

2. Device Fabrication

A heavily-doped 90nm-thick n-type GeOI wafer with 100-nm-thick buried SiO_2 and intrinsic Si was used. From secondary ion mass spectroscopy (SIMS) analysis, the average doping concentration in initial GeOI wafer was around 3×10^{18} /cm^3. The device structure of JL-FET in this work is schematically described in **Fig. 1**. First, the mesa type Ge islands were defined by wet-etching. Next, Ge islands were thinned down to 15-32 nm by a careful wet-etching (NH_3+H_2O_2+H_2O) process only for the channel regions, and 80-nm-thick Ge was remained for the S/D regions to make electrical contacts better. After cleaning with methanol and HCl, 20nm-thick-Y_2O_3 was deposited onto the Ge islands by rf-sputtering, followed by annealing at 550ºC in O_2 to passivate the surface defects. Prior to electrode formation, the sample was oxidized at low-temperature (400ºC) to form the very thin GeOx layer on S/D region, and then to weaken the Fermi-level pinning near the Ge valence band edge[4]. Finally, Al was deposited and patterned for S/D. Al was also deposited on the backside of Si as the back gate electrode. In the present work, four-point probe arrangement was prepared to subtract the parasitic resistance.

3. Results and Discussion

Fig. 2 shows transfer characteristics of Ge n-channel JL-FETs with various Ge thicknesses. The high on/off ratio of ~10^5 was achieved by thinning the thickness of Ge, so that the majority carriers in the channel were fully depleted. On the other hand, it should be noted that Ge/Al contacts at source and drain did not show the perfect ohmic characteristics in spite of the formation of pinning-relaxation layer. Therefore, we employed 4-probe measurement to estimate the channel mobility. **Fig. 3** shows the field effect mobility of Ge n-channel JL-FETs. The mobility degradation with decreasing the Ge thickness was clearly observed. Meanwhile, it is worth mentioning that the channel mobility of 32-nm-thick Ge JL-FET with subtracting the parasitic resistance is much higher than the bulk mobility in n-Si with the impurity concentration of 1-5x10^{18} /cm^3. However, the mobility in this work is lower than that in bulk n-Ge. To clarify its origin, Raman scattering measurement was carried out. FWHM of Raman peak at 300 cm^{-1} for the present GeOI was around 3.7 cm^{-1}, while it was 3.3 cm^{-1} for the conventional Ge (100) substrate. Thus, it can be concluded that the crystallinity of the present GeOI is poor than that of conventional Ge substrate, and then that Ge n-channel JL-FET has higher potential.

4. Summary

We demonstrated the high electron mobility in Ge n-channel JL-FET for the first time. The best value of field effect mobility and on/off ratio were ~1000 cm^2/Vs and 10^5, respectively. Although the S/D contact formation is a big issue to consider carefully, the channel mobility of Ge n-channel JL-FET is much higher than the bulk mobility of n-Si, which is the limitation of Si n-channel JL-FET.

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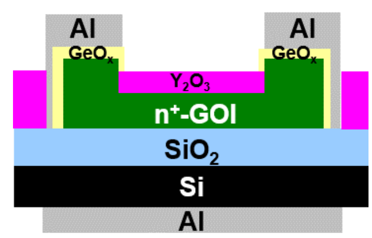

Fig. 1. The schematic of Ge n-channel JL-FET in this work. The four-point probe arrangement was prepared.

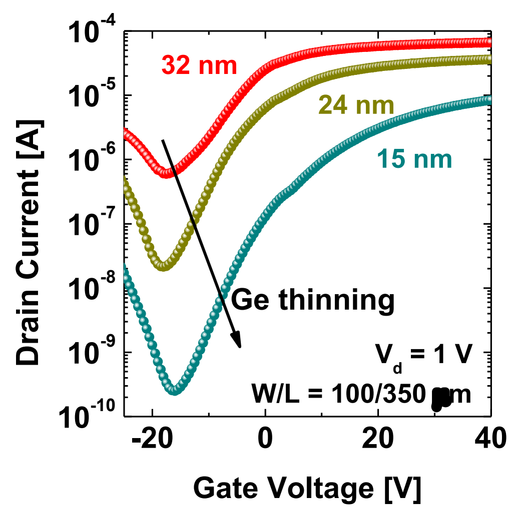

Fig. 2. Transfer characteristics of Ge n-channel JL-FETs with various Ge thicknesses.

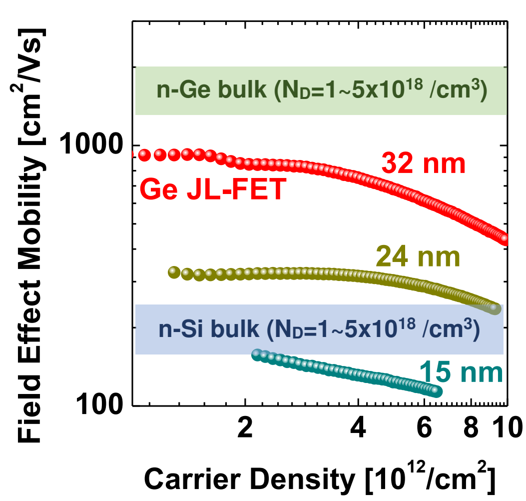

Fig. 3. The field effect mobility of Ge n-channel JL-FETs with various Ge thicknesses at V_d = 1 V, where the parasitic resistance was subtracted by performing 4-probe measurement.