Negative Capacitance Tunnel Field Effect Transistor: A Novel Device with Low Subthreshold Swing and High ON Current

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In this paper we propose a modified structure of TFET incorporating ferroelectric oxide as the complementary gate dielectric operating in negative capacitance zone, called the Negative Capacitance Tunnel FET (NCTFET). The proposed device effectively combines two different mechanisms of lowering the sub threshold swing (SS) for a transistor garnering a further lowered one compared to conventional TFET. A simple yet accurate analytical tunnel drain current model for the proposed device is also presented here. The developed analytical model demonstrates high ON current at low V_{GS} and exhibits lower SS. This paper also provides physics based explanation behind the improvement in the SS for the proposed device over TFET.

The structure of the proposed device is shown in Fig.1(b). Traditional double gate LineTFET with the high-k dielectric is the basis of this proposition. FE dielectric is assumed to be deposited on a commensurate metallic layer grown on high-k oxide. This back to back oxide structure is chosen following the experimental demonstration. The metallic layer in between oxides shields down the charge non-uniformity coming from domain formation in the FE. Fig.1(b) exhibits the ntype-NCTFET where p+ region, intrinsic region and n+ region performs the role of source, channel and drain respectively. When a gate voltage V_{GS} is applied it gets amplified by the negative capacitance action of the ferroelectric gate oxide and a higher surface potential appears in the highly doped source region as a result the semiconductor region underneath the gate becomes depleted until the appearance of inversion layer. At sufficiently high gate bias tunneling current emerges and continues to increase with the enhancement of gate voltage.

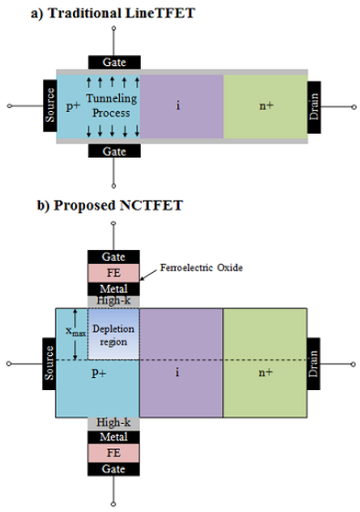

Fig. 1. (a) The TFET structure that was modeled in Ref. [1], the arrows in the highly doped source region shows the direction of band to band tunneling.(b) Simplified structure of proposed new device Negative Capacitance Tunnel FET (NCTFET)

Our model is based on the 1-D electrostatic potential variation due to the application of gate voltage. Fig. 2 shows the1-D capacitance model from the top gate to the semiconductor node in the source region along with the voltage drop across different capacitances. First, a tunnel drain current model is developed using the conventional TFET formalism which gives $I_{DS} - V_{GI}$ characteristics [1]. Then, the voltage drop across FE material V_{ins} is modeled on the basis of Ref [2] to find V_{GS}, thus completing the current (I_{DS}–V_{GS}) model for the proposed NCTFET structure.

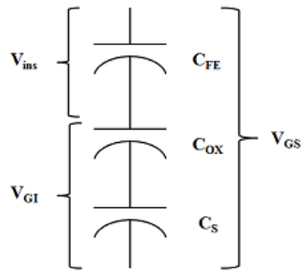

Fig. 2: 1-D capacitance model of NCTFET demonstrating the voltage drop across them.

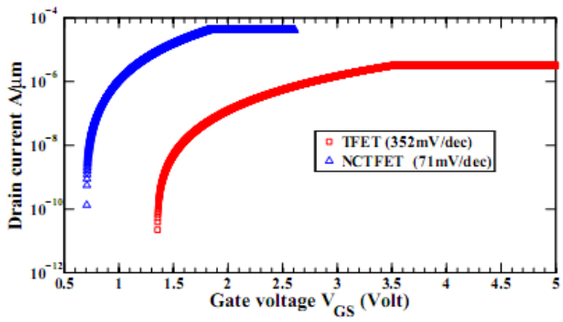

Fig. 3: $I_{DS} - V_{GS}$ characteristics of NCTFET and conventional TFET

Fig.3 shows the modeled I_{DS}-V_{GS} characteristics for NCTFET along with traditional TFET for comparison of SS. It exhibits a significant improvement in case of average subthreshold swing. Below 60 mV/dec. point swing has also been observed for this device.

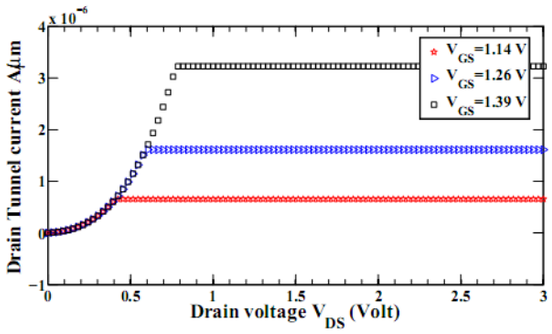

Fig. 4: Output characteristics of NCTFET with Source Doping Na = 10^{26} m^{-3} Complementary Gate dielectric($BaTiO_3$) thickness 300nm and V_{FB} = 0V

Fig.4 shows the modeled I_{DS}-V_{DS} characteristics for NCTFET which exhibits the superliner behavior.

References:

[1] J. Appl. Phys. 110, 024510 (2011)
[2] Nano Letters, vol.8, no.2, pp. 405-410, 2008.